Synopsys and GLOBALFOUNDRIES Collaborate to Deliver Design Platform and IP Enablement for 7-nm FinFET Process

Enablement Includes Industry-Leading IC Compiler II P&R Solution and DesignWare Embedded Memory IP

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Highlights:

- Synopsys Design Platform supports advances in GLOBALFOUNDRIES' 7-nm low-power technology and Self-Aligned Double Patterning (SADP)
- IC Compiler II enhancements include router advancements tuned to realize power-performance benefits of the 7-nm process
- Familiar flow steps enhanced to meet new 7-nm requirements and implemented on design example including high performance memories
- High-speed, high-density, ultra-density DesignWare Memory Compilers and HPC Design Kits deliver superior performance, power and area

Synopsys, Inc. (Nasdaq: SNPS) today announced the enablement of the Synopsys Design Platform and DesignWare® Embedded Memory IP on GLOBALFOUNDRIES 7-nm Leading-Performance (7LP) FinFET process technology. Synopsys and GF collaboration on the new process addressed several new challenges specific to the 7LP process. This process is expected to deliver 40 percent more processing power and twice the area scaling compared to GF's 14nm FinFET process. Designers of premium mobile processors, cloud servers and networking infrastructure can take advantage of these benefits by confidently deploying the silicon-proven Synopsys Design Platform and Embedded Memory IP.

"GF's leading-performance 7-nm platform is exceeding initial performance targets and is now ready for customer designs," said Alain Mutricy, senior vice president of product management at GF. "GF and Synopsys have collaborated to provide designers with tools and methodology that fully leverage the power and highest absolute performance of our 7LP technology, and will allow customers to create innovative products across a range of high-performance applications."

GF and Synopsys worked together to ensure support of the comprehensive suite of Synopsys Design Platform digital implementation solutions for GF 7LP, including Design Compiler® Graphical synthesis, IC Compiler™ II place-and-route, IC Validator physical verification, PrimeTime® static timing analysis and StarRC™ extraction. To enable designers to achieve the full benefit of the GF 7LP process, the Synopsys tools employ advanced techniques including color track generation, pin color alignment checking and legalization, mixing of single-height and double-height physical boundary cells, power grid alignment to track and color-track aware routing.

The two companies are also collaborating on the development of Synopsys DesignWare Memory Compilers to deliver leading performance, power, area and yield for GF's 7-nm process technology. This joint effort consists of optimizing the GF 7LP process design rules and line patterns to achieve the best results. Early versions of the memory compilers will be on the GF 7LP process qualification vehicle.

"Synopsys and GF have always worked closely to address our customers' needs, including collaborations on FDSOI and 14-nm FinFET processes," said Michael Jackson, corporate vice president of marketing and business development in the Design Group at Synopsys. "With today's announcement, we are ready to enable designs on the 7LP process. We will continue to collaborate and ensure that our customers can get superior quality of results and faster time to results by using the Synopsys Design Platform and DesignWare Embedded Memory IP."

Availability

Support for Synopsys Design Platform is available today for GF process technologies. The DesignWare Embedded Memory and Interface IP for the GF 7LP process are in development. For more information on the collaboration between GF and Synopsys, please visit www.globalfoundries.com

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and

semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected release and benefits of the DesignWare Embedded Memory and Interface IP for the GLOBALFOUNDRIES 7LP processes. Any statements that are not statements of historical fact may be deemed to be forward-looking statements. These statements involve known and unknown risks, uncertainties and other factors that could cause actual results, time frames or achievements to differ materially from those expressed or implied in the forward-looking statements. Other risks and uncertainties that may apply are set forth in the "Risk Factors" section of Synopsys' most recently filed Quarterly Report on Form 10-Q. Synopsys undertakes no obligation to update publicly any forward-looking statements, or to update the reasons actual results could differ materially from those anticipated in these forward-looking statements, even if new information becomes available in the future.

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