# Synopsys Integrates VESA Display Stream Compression into DesignWare MIPI DSI IP to Enable 4K Ultra HD and Higher Resolution Displays

Complete Compliant MIPI Display Solution Reduces Data Transmission Bandwidth for Mobile, Virtual Reality and Automotive SoCs

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**Highlights:**

- Complete DesignWare MIPI DSI Host Controller with VESA DSC encoder and MIPI D-PHY easily integrates into application processors with less risk
- Integrated MIPI display IP reduces memory size and data transmission bandwidth to lower power consumption and area
- VESA DSC encoder allows higher refresh rates beyond 60Hz for drastically faster responsiveness and fluidity in ultra-high-resolution quad HD or 4K displays

Synopsys, Inc. (Nasdaq:SNPS) today announced its integrated DesignWare® MIPI DSI Host Controller IP with the Video Electronics Standards Association (VESA®) Display Stream Compression (DSC) encoder, delivering a complete display IP solution for mobile, augmented/virtual reality and automotive SoCs. The IP supports ultra-high-resolution quad HD or 4K displays with refresh rates at 60Hz or higher for both image and video, enabling faster frame responsiveness and more display fluidity. The integrated IP reduces memory size and data transmission bandwidth to lower power consumption, area and electromagnetic interferences (EMI). The DesignWare MIPI DSI Host Controller IP with VESA DSC encoder together with DesignWare MIPI D-PHY IP provide designers with a complete, interoperable solution for integration into application processors.

"The demand for 4K and higher resolution displays for high-end smartphones and new applications like virtual/augmented reality, automotive infotainment and advanced driver assistance systems (ADAS) is growing," said Joel Huloux, chairman of the board of MIPI Alliance. "As a MIPI Alliance board member and contributor to the Display Working Group, Synopsys continues to promote interoperability within the ecosystem and drive adoption of the MIPI DSI specification for high-definition displays in mobile applications and beyond."

"Display manufacturers for mobile, IoT and automotive applications are moving to higher-resolution displays to differentiate their products, challenging SoC designers to find methods to compress data transmission for increased pixel count," said Bill Lempesis, executive director at VESA. "By integrating the DSC encoder with its DesignWare MIPI DSI Host Controller IP, Synopsys is providing designers the opportunity to incorporate visually lossless compression over display links into their SoCs."

The DesignWare MIPI DSI Host Controller IP with the VESA DSC encoder is configurable from 1 to 4 lanes, extending the bandwidth up to a total of 30 Gbps for 4K resolution displays. For a more flexible implementation, the integrated DSC encoder supports input and output RGB formats with 8 or 10 bits per component as well as single or multiple slices as defined by the VESA DSC specification. The DSC encoder is fully verified in a universal verification methodology (UVM) environment and checked against the VESA DSC v1.1 C model using a comprehensive test image library, providing designers with a highly integrated, verified and low-risk solution.

"The growing demand for ultra-high-resolution mobile displays with wider picture range, broader color range and better contrast ratios in consumer devices brings new challenges to SoC designers," said John Koeter, vice president of marketing for IP at Synopsys. "Synopsys' DesignWare MIPI DSI Host Controller IP with integrated VESA DSC encoder enables designers to meet the requirements for quad HD, 4K and higher resolution display with higher refresh rates for the next generation of mobile displays."

**Availability and Additional Resources**

Available now:

- DesignWare MIPI DSI Host Controller IP with VESA DSC encoder
- DesignWare MIPI D-PHY IP
- DesignWare MIPI DSI Host Controller IP

For more information, visit DesignWare MIPI IP solutions website.

**About DesignWare IP**

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit https://www.synopsys.com/designware.

**About Synopsys**

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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