Synopsys' New Superscalar ARC HS Processors Boost RISC and DSP Performance for High-End Embedded Applications

DesignWare ARC HS4x Family Delivers Twice the Signal Processing Performance of Previous ARC HS Cores with Integrated DSP Capability

Disclaimer: GlobalFoundries acquired the Synopsys Processor Solutions business on June 1, 2026. Clickhere to learn more.

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Highlights:

- New ARC HS4x and HS4xD processors with dual-issue architecture increase RISC performance by 25 percent compared to the popular ARC HS3x family while adding 2x higher DSP performance with energy efficient signal processing for wireless baseband, voice/speech, mid-range audio and embedded DSP applications
- ARC HS4xD processors implement the extensible ARCv2DSP Instruction Set Architecture (ISA) with more than 150 DSP instructions to accelerate signal processing algorithms
- MetaWare Development Toolkit makes the ARC processors easy to program and offers enhanced support for dual-issue architecture and DSP hardware, maximizing performance and minimizing code size
- Multicore configurations support up to four cores with L1 coherency and L2 cache for higher performance processing

Synopsys, Inc. (Nasdaq: SNPS) today announced availability of the new DesignWare® ARC® HS4x and HS4xD processor family for high-performance embedded applications. The ARC HS44, HS46, HS48, HS45D and HS47D processors, available in single-, dual- and quad-core configurations, implement a dual-issue superscalar architecture that delivers up to 6000 DMIPS per core, making it the highest performance processor in the popular ARC HS family. The HS45D and HS47D also support more than 150 DSP-optimized instructions, delivering 2x higher performance and a unique combination of high-performance control and high-efficiency digital signal processing. To make it easier to take advantage of the new hardware features and simplify software development, the MetaWare Development Toolkit has been enhanced with dual-issue pipeline support, a rich DSP software library and an optimized C/C++ compiler. The ARC HS4x and HS4xD processors are designed to meet the power, performance and area requirements of a broad range of high-end embedded applications including solid-state drives (SSDs), wireless baseband, wireless control, home networking, automotive control and infotainment, multi-channel home audio, advanced human-machine interface (HMI), industrial control and home automation.

"Our design team is under constant pressure to achieve higher performance for our SSD controllers to keep up with the rapidly evolving enterprise market," said Sky Shen, CEO at Starblaze. "Synopsys' new ARC HS4x and HS4xD processors will enable us to achieve new levels of performance while limiting power consumption and chip area, which is very important in our application. Additionally, the ARC development tools and ecosystem will help us accelerate our software development effort and project schedules."

"A growing number of embedded applications require a combination of high-performance RISC execution and energy-efficient signal processing," said Linley Gwennap, principal analyst at The Linley Group. "Synopsys' new HS4xD processors, with their superscalar architecture and hardware DSP support, give SoC designers an alternative to implementing separate CPU and DSP cores, saving power and silicon gates."

Dual-Issue HS4x Family for High-End Control and Embedded Linux Capabilities

The ARC HS44, HS46 and HS48 processors utilize the ARCv2 instruction-set architecture (ISA), which enables the implementation of high-performance embedded designs with low power consumption and a small silicon footprint. The ARC HS4x family features a high-speed 10-stage, dual-issue pipeline that supports out-of-order execution, minimizing idle processor cycles and maximizing instruction throughput. The processors deliver up to 6000 DMIPS per core at 2.5 GHz while requiring only 0.06 mm^2 of area and as little as 37 microwatts/MHz in typical 16-nm FinFET processes. The sophisticated branch prediction and a late-stage ALU reduce load-to-use latency to improve instruction processing efficiency. The HS4x processors are available in single-, dual- and quad-core configurations that deliver up to 24,000 DMIPS per cluster. The HS46 and HS48 offer instruction and data caches (up to 64 KBs of each) and support for full Level 1 (L1) cache coherency. The HS48 also incorporates up to eight megabytes of Level 2 (L2) cache as well as a full-featured memory management unit (MMU) supporting symmetric multiprocessing (SMP) Linux. Like all ARC processors, all HS4x processors are configurable and implement the ARC Processor EXtension (APEX) technology that enables the addition of custom instructions to meet the unique performance, power and area requirements of each target application.

High-Efficiency DSP with the HS4xD Family

The HS45D and HS47D offer the same high-end control features of their HS4x counterparts with additional DSP capabilities useful for baseband, audio, voice, speech and other signal processing applications. To speed the execution of math functions, the HS45D and HS47D give designers the option to implement a hardware integer divider, instructions for 64-bit multiply, multiply-accumulate (MAC), vector addition and vector subtraction, and a configurable IEEE 754-compliant floating point unit (single- or double-precision or both). The ARC HS4xD processors are compatible with the ultra-low power ARC EMxD processors and have the same instruction set, making it easy to migrate code between the two processor families.

The blend of high-performance RISC and DSP capabilities in the HS4xD processors provides efficient multi-channel audio processing for mobile, home and automotive infotainment applications. The HS4xD can simultaneously manage control tasks such as communications stacks and filesystem support while providing the signal processing bandwidth to support audio decoding, post-processing and voice-based HMI processing. These tasks are critical to high-performance wireless streaming speaker systems and voice-activated assistants found in an increasing number of homes. A portfolio of HS4xD-optimized audio/voice codecs and post-processing software is available from Synopsys and third-party partners.

MetaWare Development Toolkit Eases HS4x/HS4xD Processor Programming

The ARC HS4x and HS4xD Processor family is supported by a robust ecosystem of software and hardware development tools, including the MetaWare compiler/debugger, the nSIM instruction set simulator, the MQX real-time operating system (RTOS), and third-party tools, operating systems (including Linux) and middleware from leading industry vendors. The MetaWare Development Toolkit includes an optimized library of DSP functions such as FFT and DCT, FIR and IIR filters, as well as vector and matrix math functions, allowing software engineers to rapidly implement algorithms from standard DSP building blocks. The Toolkit also includes an ITU-T base-ops library for developing voice codecs. For regular C code, the compiler automatically generates ARCv2DSP ISA instructions to deliver the best performance, including guided and auto vectorization optimizations.

"We are seeing tremendous innovation and increasing complexity in embedded applications such as SSDs, wireless control and home networking, which is driving the need for significant performance increases in embedded processors," said John Koeter, vice president of marketing for IP at Synopsys. "The new ARC HS4x and HS4xD processors are the highest performance processors in the ARC portfolio, enabling designers to address the growing control and signal processing demands for their embedded designs."

Availability & Resources

The ARC HS44, HS46, HS48, HS45D and HS47D processors are scheduled to be available in June 2017.

Learn more about the DesignWare ARC HS4x/HS4xD Processors:

- ARC HS44, HS46, HS48 Processors
- ARC HS45D and HS47D Processors

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected release and benefits of the ARC HS44, HS46, HS48, HS45D and HS47D processors. Any statements that are not statements of historical fact may be deemed to be forward-looking statements. These

statements involve known and unknown risks, uncertainties and other factors that could cause actual results, time frames or achievements to differ materially from those expressed or implied in the forward-looking statements. Other risks and uncertainties that may apply are set forth in the "Risk Factors" section of Synopsys' most recently filed Quarterly Report on Form 10-Q. Synopsys undertakes no obligation to update publicly any forward-looking statements, or to update the reasons actual results could differ materially from those anticipated in these forward-looking statements, even if new information becomes available in the future.

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