Synopsys Delivers Industry's First Multi-Protocol 25G PHY IP in 7-nm FinFET Process

DesignWare PHY IP Cuts Power and Area by More Than 35 Percent for High-Performance Computing Applications Including Machine Learning and Artificial Intelligence

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Highlights:

- DesignWare Multi-Protocol 25G PHY supports protocols including PCI Express, Ethernet, SATA and new Cache Coherent Interconnect for Accelerators (CCIX)
- Compact PHY IP with advanced power management features significantly reduces active power consumption
- Programmable continuous calibration and adaptation algorithms optimize performance across voltage and temperature variations for networking and computing applications
- Support for chip-to-chip, port side and backplane interfaces eases system-level integration

Synopsys, Inc. (Nasdaq: SNPS) today announced its new DesignWare® Multi-Protocol 25G PHY IP for high-performance computing applications including machine learning and artificial intelligence. The PHY IP gives designers the flexibility to efficiently integrate multiple protocols including PCI Express® 4.0, 25G Ethernet, SATA and CCIX into system-on-chips (SoCs) targeting the 7-nanometer (nm) and 16-nm FinFET processes. The multi-protocol 25G PHY reduces power and area by more than 35 percent compared to the 16G PHY solution, incorporating optional power management features such as I/O supply under drive and decision feedback equalization (DFE) bypass. In addition, the programmable continuous calibration and adoption (CCA) feature optimizes performance across voltage and temperature variations, which is critical in harsh data center environments. Designers can integrate the multi-protocol 25G PHY with Synopsys' digital controllers and verification IP for a complete, low latency, power-efficient IP solution that is compliant with the industry-standard protocol specifications.

"Globally, peak Internet traffic is projected to increase 4.6x from 2016 to 2020, a 36 percent CAGR, requiring semiconductors to incorporate new capabilities to meet high bandwidth demands of data center SoCs. The average number of IP blocks in these SoCs was 151 in 2016 and is projected to grow to 246 by 2020," said Richard Wawrzyniak, principal analyst at Semico Research and Consulting Group. "Semico foresees the main enablers for high data rates to be high-speed SerDes solutions such as Synopsys' new optimized DesignWare Multi-Protocol 25G PHY IP."

DesignWare Multi-Protocol 25G PHY IP offers unique features to help designers meet their complex design requirements, including:

- Flexible clock multiplier unit (CMU) including dual PLLs and dividers to support flexible multi-protocol configurations while transmitting high-quality data across lossy channels
- Performance analog front-end that incudes adaptive continuous time linear equalizer (CTLE), decision feedback equalization (DFE) and feed forward equalization (FFE) for superior signal integrity and jitter performance
- Embedded bit error rate (BER) circuitry to efficiently evaluate channel quality, and on-die test features for testability and visibility into system performance, without requiring external test equipment

"The increase in global data traffic due to the growth of connected devices is requiring faster data

transmission over the network," said John Koeter, vice president of marketing for IP at Synopsys. "The DesignWare Multi-Protocol 25G PHY addresses the high bandwidth and quality of service requirements for high-performance computing SoCs that require a wide range of interconnect protocols."

Availability & Additional Resources

The DesignWare Multi-Protocol 25G PHY IP full silicon design kit for TSMC's 7-nm FinFET process is available now. The full silicon design kit for the Multi-Protocol 25G PHY IP in TSMC's 16-nm FinFET process is scheduled to be available in October of 2017.

Learn more about DesignWare Multi-Protocol 25G PHY IP, download the datasheet.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected release and benefits of DesignWare Multi-Protocol 25G PHY IP for 16-nm FinFET processes. Any statements that are not statements of historical fact may be deemed to be forward-looking statements. These statements involve known and unknown risks, uncertainties and other factors that could cause actual results, time frames or achievements to differ materially from those expressed or implied in the forward-looking statements. Other risks and uncertainties that may apply are set forth in the "Risk Factors" section of Synopsys' most recently filed Quarterly Report on Form 10-Q. Synopsys undertakes no obligation to update publicly any forward-looking statements, or to update the reasons actual results could differ materially from those anticipated in these forward-looking statements, even if new information becomes available in the future.

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