Synopsys IC Validator Physical Signoff Verifies 10 Billion+ Transistors Within Hours

Massively Parallel Architecture Accelerates Physical Signoff and Delivers Industry-Leading Turnaround Time

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Highlights:

- Latest releases of IC Validator deliver 2x higher capacity and 2x smaller disk usage
- Proven scalability with excellent distributed processing and multi-threading delivers industry-leading physical signoff turnaround time for the world's largest designs
- Lockstep close collaboration with foundries provides runset access to early technology node adopters

Synopsys, Inc. (Nasdaq: SNPS) today announced that its IC Validator was successfully deployed on some of the industry's largest and most advanced designs to accelerate design rule checking (DRC) closure. Through near-linear distributed processing and efficient resource management, IC Validator delivers industry-leading turnaround time, enabling physical signoff within hours on designs with 10 billion+ transistors. Technology advancements in the latest releases of IC Validator reduce both memory and disk usage requirements by 2x. This significant improvement in resource efficiency enables excellent performance scaling to several hundreds of CPUs by taking advantage of the smaller and more readily available machines in the customers' existing compute farms.

"Increasing manufacturing complexity at advanced nodes makes it challenging for customers to complete physical signoff within schedule," said Bijan Kiani, vice president, product marketing, Design Group at Synopsys. "Through high-performance scalability and readily available, optimized runsets from all major foundries, IC Validator is providing our customers with the fastest path to production silicon."

IC Validator, part of the Synopsys Digital Design Platform, is a comprehensive and highly scalable physical signoff solution including DRC, LVS, programmable electrical rule checks (ERC), dummy fill and DFM enhancement. IC Validator is configured for today's extremely large designs by enabling 8 CPUs with a single license. It uses both multi-threading and distributed processing over multiple machines to provide near linear scalability benefits that extend to several hundreds of CPUs. IC Validator enables coding at higher levels of abstraction and is architected for scalability to maximize utilization of mainstream hardware, using smart memory-aware load scheduling and balancing technologies.

IC Validator is a companion product to Synopsys IC Compiler™ II In-Design physical signoff. In-Design allows place-and-route engineers to perform independent signoff-quality analysis earlier, before the design is finalized and while correction can be automated. In-Design technology enables new high-productivity functionality within the place-and-route environment, including automatic DRC repair, improved timing quality-of-result with timing-aware metal fill, and rapid ECO validation. In-Design physical signoff eliminates expensive iterations with downstream analysis tools and maintains a convergent design flow to physical signoff.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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