Synopsys' IC Validator Used for Physical Sign-Off on More Than 100 FinFET Production Tapeouts

Industry leaders in CPU, GPU and fabless SoC markets adopt IC Validator's massively parallel distributed processing for overnight signoff

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Highlights:

- Industry's most complex chips verified with more than 200 CPUs overnight
- Complete foundry runset coverage for all FinFET processes
- In-Design physical signoff with IC Compiler II place-and-route system for rapid ECO flow

Synopsys, Inc. (Nasdaq: SNPS) today announced that its IC Validator physical verification product has been successfully used for signoff on more than 100 tapeouts at advanced FinFET nodes. These tapeouts were completed with process technologies from multiple foundries at 16nm, 14nm, 10nm and 7nm. IC Validator's massively parallel scalability to more than 200 CPUs has proven a critical factor in its ability to deliver overnight run times for today's highly complex technology rules and very large designs. Synopsys has cooperated closely with foundries for several years to ensure the uncompromising accuracy of IC Validator's results. This dependable accuracy has been key to IC Validator's growing list of successful adoptions by industry leaders in many markets ranging from top CPU and GPU design companies in the US to leading fabless SoC designers in Taiwan and Japan.

IC Validator, part of the Synopsys Galaxy™ Design Platform, is a comprehensive and highly scalable physical verification tool suite including DRC, LVS, programmable electrical rule checks (ERC), dummy fill and DFM enhancement. IC Validator is configured to meet the challenges of today's extremely large designs by enabling 8 CPUs with a single license. It uses both multi-threading and distributed processing over multiple machines to provide scalability benefits that extend to more than 200 CPUs. IC Validator enables coding at higher levels of abstraction and is architected for near-linear scalability that maximizes utilization of mainstream hardware, using smart memory-aware load scheduling and balancing technologies.

IC Validator is a companion product to the IC Compiler™ II place-and-route system for In-Design physical verification. In-Design is enabled by the intelligent integration of IC Validator and IC Compiler II place-and-route, making it possible for engineers to perform independent signoff-quality analysis earlier, before the design is finalized and while correction can be automated. In-Design technology also enables new high-productivity functionality within the place-and-route environment, including automatic DRC repair, improved quality of timing results with timing-aware metal fill, and rapid ECO validation. In-Design physical verification eliminates expensive iterations with downstream analysis tools and maintains a convergent design flow to physical signoff.

"As manufacturing complexity is placing increased challenges on designers to deliver within schedule, it is extremely important that we continue to collaborate closely with leading foundries to deliver high-performance solutions," said Bijan Kiani, vice president, product marketing, Design Group at Synopsys. "This milestone confirms our mature ecosystem strategy that has led to strong growth in IC Validator's market share."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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