Synopsys Announces Availability of Comprehensive Low Power Reference Kit for Design and Verification

Bitcoin-mining Design-based Kit Features Complete RTL-to-GDSII Low Power Methodology

MOUNTAIN VIEW, Calif., March 21, 2017 /PRNewswire/ --

Highlights:

- Showcases Synopsys' comprehensive low power flow on a real-world design
- Demonstrates a flexible methodology to rapidly deploy advanced low power techniques
- Includes RTL, constraints, UPF power intent, test benches, documentation and all scripts spanning verification, implementation and signoff tools

Synopsys, Inc. (Nasdaq: SNPS) today announced the immediate availability of a comprehensive low power reference kit for design and verification based on a bitcoin mining System-on-Chip (SoC) design. The detailed low power flow and accompanying reference kit covers all aspects of a typical SoC design flow, methodically stepping through all phases from RTL creation through final signoff. It is specifically designed to help accelerate deployment of a Unified Power Format (UPF)-based hierarchical design methodology by providing all design views with built-in templates and scripts spanning more than 15 Synopsys products.

The low power reference kit can also be used as an integrated learning vehicle for the complete Synopsys low power flow. Modular in nature, it easily helps with incremental adoption of a specific or broader-range of tools, allowing project teams to concentrate on particular functional areas such as verification or implementation.

The reference kit includes a user guide that provides step-by-step instructions for the individual tools used during various stages of a low power design flow.

"Power efficiency is a key imperative in design where engineers are using complex and advanced strategies to minimize SoC power consumption," said Godwin Maben, reference kit architect and scientist for Synopsys' Design Group. "The Synopsys low power reference kit encapsulates the complex techniques in an easy to deploy, silicon-proven flow using market-leading implementation and verification tools from Synopsys."

Key Synopsys products covered by the low power reference kit include:

- IC Compiler™ II place and route system
- Design Compiler ® RTL synthesis product family
- DFTMAX™ and TetraMAX® II test solutions
- Formality® formal verification tool
- PrimeTime® and PrimeTime PX timing and power signoff
- StarRC™ extraction solution
- VCS® native low power simulation
- Verdi® automated debug system
- SpyGlass ® static verification tool
- VC LP low power static verification

Availability

The Synopsys low power reference kit will be launched at a special verification and implementation session titled "A Completely Cool Case Study" at the Synopsys User's Group (SNUG®) event – Silicon Valley's largest technical conference – on March 23, 2017 in Santa Clara, CA. Register to attend the session at the Santa Clara Convention Center. The "Low Power Flow Reference Design Kit" will be available for download following the session at https://solvnet.synopsys.com/retrieve/2630223.html

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP, and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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