

Synopsys' IC Compiler II Completed Certification for TSMC's 7-nm Process Technology

TSMC certifies 7-nm Synopsys Galaxy Design Platform suite of digital, Signoff, Custom, and AMS Tools

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Highlights:

- Design Compiler Graphical and IC Compiler II support for TSMC's innovative Via Pillar flow for high-performance computing (HPC) designs
- Low voltage design is enabled by advanced waveform propagation and parametric on chip variation technologies in the Galaxy Design Platform
- Custom Compiler certification of TSMC's 7-nm process technology

Synopsys, Inc. (Nasdaq: SNPS) today announced that TSMC has certified the Synopsys Galaxy™ Design Platform for the V1.0 of its latest 7-nanometer (nm) FinFET process technology.

Further collaborations, anchored around the Design Compiler® Graphical and IC Compiler™ II digital implementation products, have supported TSMC's High Performance Compute (HPC) methodology to mutual customers for the 7-nm node that is proven to deliver broad performance gains aimed at compute-intensive designs. The results of this joint collaborative work will accelerate designers' creation of next generation products.

With process, performance and yield demands requiring innovative solutions, a broad collaboration on via-structures, seamlessly supported throughout the flow, is a key part of both 7-nm design and the 7-nm HPC flow deployment. The solution consists of performance exploration and what-if analysis of via-structures through Design Compiler Graphical as well as automatic creation and insertion in the IC Compiler II place-and-route flow coupled with PrimeTime ECO support that preserves and enhances via-pillar structures during final timing-signoff ECO stages. The Synopsys-TSMC collaboration produces innovative methodology to enable 7-nm high-performance, high-reliability designs.

Addressing the needs of low-power operation, low-voltage enablement is delivered throughout the Galaxy Design Platform with comprehensive support for Advanced Waveform Propagation (AWP) allied with Parametric-on-chip-variation (POCV) technologies.

IC Compiler II additionally brings signoff timing accuracy within the design-closure phase through the deployment of the PrimeTime® timing analysis and signoff technology. A platform-wide deployment of Total-Power-Optimization technologies, including expanded multi-bit-methodology support and advanced concurrent-clock-and-data optimization, furthers designers' ability to deliver highly differentiated, low-power products.

PrimeTime physically-aware ECO has been enhanced for 7-nm, seamlessly accounting for the latest process-driven requirements, including pin-track alignment of ECO placed cells and power recovery for lower leakage.

"This signifies the completion of long collaboration between Synopsys and TSMC to deliver full flow design tools and collateral at 7-nm process technology," said Suk Lee, TSMC senior director, Design Infrastructure Marketing Division. "The results of the partnership enable designers to begin early tapeouts today."

"The collaboration takes full advantage of innovative TSMC 7-nm high-performance low power technologies," said Bijan Kiani, vice president of product marketing for the Design Group at Synopsys. "The end result enables our mutual customers to engage immediately on high quality production 7-nm designs using the Galaxy Design Platform."

The Galaxy tools certified by TSMC for their 7-nm process include:

- IC Compiler II place and route: full-color routing and extraction, advanced cut-metal modeling for reducing end of line spacing, and a full flow deployment of Via Pillar technology.
- PrimeTime signoff timing: Signoff accurate timing analysis with enhanced variation modeling, low voltage support and Via Pillar ECO technology for HPC designs
- StarRC™ signoff extraction: Advanced color-aware variation modeling, Via Pillars support for high-performance design and enhanced FinFET MEOL parasitic modeling for needed accuracy
- IC Validator physical signoff: Certified runsets for signoff DRC and LVS; cut-metal and complex fill-to-signal space support
- HSPICE®, CustomSim™ and FineSim® simulation solutions: FinFET device modeling with self-

heating/aging effect and Monte Carlo feature support. Accurate circuit simulation results for analog, logic, high-frequency, and SRAM designs.

- Custom Compiler custom design: Full coloring interactive routing, DRC checks and density reporting, color-aware EM and RC reporting.
- NanoTime custom timing analysis: SPICE-accurate transistor-level static timing analysis of 7-nm embedded SRAMs, with new mesh network parasitic modeling of power rail trench contacts.
- ESP-CV custom functional verification: Transistor-level symbolic equivalence checking for 7-nm SRAM, macros, and library cell designs.
- CustomSim reliability analysis: Accurate dynamic transistor-level IR/EM analysis for color-aware EM rules and advanced via support.
- In addition, gate-level static/dynamic signal and PG IR/EM analysis with advanced cell current distribution modeling has been implemented in PrimeRail, not including thermal-aware capability which is an on-going collaboration between TSMC and Synopsys.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP, and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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