Synopsys Advances Virtual Prototyping to Enable System and Semiconductor Supply Chain Collaboration for Next-Generation SoCs

New Task Graph Generation Technology in Synopsys Platform Architect Automates Capture of Key Performance Requirements Needed to Explore Next Generation SoC Architectures

MOUNTAIN VIEW, Calif., March 8, 2017 /PRNewswire/ -- **Highlights:**

- System companies and their semiconductor suppliers are adopting virtual prototyping to align on architecture specifications for next generation SoCs
- Predicting the performance and power of next generation SoC architectures requires an understanding of the processing and communication characteristics of the application
- Task graphs describe these characteristics for early analysis and efficient exploration of candidate SoC architectures for performance and power
- New Task Graph Generator in Synopsys Platform Architect automatically creates task graphs from target software applications such as operating systems, web browsing image capture and video playback
- Task graphs enables system and semiconductor companies to more easily hand off requirements through the supply chain

Synopsys, Inc. (Nasdaq: SNPS) today announced the availability of a key technology in virtual prototyping which enables architecture performance requirements to be easily shared through the supply chain. The latest release of its Platform Architect™ solution introduces new Task Graph Generator (TGG) technology, which automatically extracts key performance characteristics from software applications to enable architecture exploration to optimize performance and power for next generation multicore system-on-chips (SoCs). TGG enables system architecture teams to more easily share accurate application workload models with their semiconductor suppliers, enabling much more efficient collaboration in the supply chain.

"To address growing software content, the use of multicore architectures in automotive electronic systems is increasing," said Takashi Abe, project manager, Basis Electronics R&D Division at Denso. "Using the TGG capability in Platform Architect, we are able to capture the key characteristics of our existing software and derive the performance of next generation multicore architectures with high accuracy. By applying this approach early in the planning phase, we are able to ensure that system specifications will meet the demanding performance requirements of these applications."

Using Platform Architect, semiconductor suppliers can define the architecture specification for next generation SoCs based on the software application requirements from their system customers. System designers can map a software workload model generated by TGG, called a task graph, to the processing resources in the SoC. This allows them to explore, analyze and optimize the performance and power of next generation multicore SoC architectures very early in the development cycle. And, because task graphs are abstract workload models and not the actual software, systems design teams can more easily share them with their semiconductor suppliers as executable specifications, benefiting collaboration in the supply chain.

TGG is application profiling technology that takes software execution traces as its input. By running the application program of interest on an existing system, designers can record their input using a supported TGG format, including:

- OS-level traces for programs executing on any Linux, Android, and QNX based system, including existing hardware devices
- Function-level traces for programs executing on x86 based systems (Windows or Linux), using the Pin instrumentation tool from Intel, and on ARM-based systems using Synopsys Virtualizer Development Kit (VDK) virtual prototypes or ARM® DS-5 Development Studio

TGG analyzes the execution trace to extract the processing and communication requirements of the application of interest, including task level parallelism and dependencies, processing cycles per task, and read/write memory accesses, to generate the resulting task graph workload model for performance analysis and benchmarking of new architectures in Platform Architect.

"Delivering the right balance of performance and energy efficiency is critical to avoid under- and over-design," said Eshel Haritan, vice president, virtual prototyping R&D for the Synopsys Verification Group. "With Task Graph Generator in Platform Architect, system designers gain a realistic, system-level benchmark view of critical SoC applications, enabling system design teams to explore and optimize the performance and power of their new architecture months before final hardware and software are available, reducing risk and improving

results."

Availability & Resources

Platform Architect with TGG technology is available now from Synopsys.

- Learn more about Platform Architect MCO: http://www.synopsys.com/platformarchitect

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Editorial Contacts:
Carole Murchison
Synopsys, Inc.
650-584-4632
carolem@synopsys.com

SOURCE Synopsys, Inc.