Synopsys Announces Industry's First ASIL D Ready Dual-Core Lockstep Processor IP with Integrated Safety Monitor

New ARC EM Safety Islands Simplify Development and Accelerate ISO 26262 Certification of Advanced Driver Assistance Systems, Radar and Sensor Applications

Disclaimer: GlobalFoundries acquired the Synopsys Processor Solutions business on June 1, 2026. Clickhere to learn more.

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Highlights:

- ARC EM Safety Islands are pre-built, verified and ASIL D Ready certified dual-core lockstep processors with integrated safety monitors, reducing the design effort to achieve the highest automotive safety level
- Operates in either lockstep mode for ASIL D applications or independent dual-core mode to optimize performance for ASIL B applications
- Tightly-coupled interrupt controller, microDMA and memory protection unit on each core provide full redundancy
- ASIL D Ready certified ARC MetaWare Compiler accelerates development of ISO 26262-compliant software

Synopsys, Inc. (Nasdaq: SNPS) today announced availability of DesignWare® ARC® EM Safety Island IP, dual-core lockstep processors that simplify development of safety-critical applications and accelerate ISO 26262 certification of automotive system-on-chips (SoCs). The new Automotive Safety Integrity Level (ASIL) D Ready certified DesignWare ARC EM4SI, EM6SI, EM5DSI and EM7DSI processors integrate a self-checking safety monitor as well as hardware safety features such as error correcting code (ECC) and a programmable watchdog timer to help detect system failures and runtime faults. The ARC EM Safety Islands are supported by comprehensive safety documentation, including failure modes, effects and diagnostic analysis (FMEDA) reports that facilitate chip- and system-level ISO 26262 ASIL D compliance. In addition, the ASIL D Ready certified ARC MetaWare Development Toolkit for Safety eases the development, debugging and optimization of ISO 26262-compliant software targeting ARC processors. The ARC EM Safety Islands are designed to meet the area and safety requirements of a broad range of automotive applications including advanced driver assistance systems (ADAS), radar and sensors.

"Eliminating single points of failure in safety-critical SoCs is paramount to achieving ASIL D certification," saidWolfgang Ruf, product manager, semiconductors at SGS-TÜV Saar GmbH. "By using Synopsys' pre-verified ASIL D Ready certified ARC EM Safety Islands, designers can significantly reduce the development effort and time needed to achieve ISO 26262 certification for their automotive SoCs."

The DesignWare ARC EM Safety Islands are configurable and extendable to meet the unique performance, power and area requirements of each target application. The ARC EM4SI is a dual-core lockstep processor solution based on the 32-bit ultra-compact ARC EM4 processor with single-cycle closely coupled memories. The ARC EM5DSI, based on the ARC EM5D processor, adds more than 150 DSP instructions and a unified multiply/MAC unit to accelerate signal processing algorithms. The ARC EM6SI and ARC EM7DSI offer the same functionality as the EM4SI and EM5DSI, respectively, and include up to 32 KB of instruction and data caches. The ARC EM Safety Islands include a range of safety-related features including:

- Self-checking safety monitor to ensure lockstep operation
- ECC logic to identify and correct data and address errors on closely coupled memories
- Hardware stack protection checks for overflow and underflow of reserved stack space to prevent data corruption and program crashes
- Integrated watchdog timer to help recover from a deadlock situation and enable countermeasures in case of tampering

The safety monitor also includes time diversity with parity to protect system integrity if noise pulses hit both cores simultaneously. Options to the ARC EM Safety Islands include a floating point unit (FPU), a microDMA controller as well as a memory protection unit (MPU) to help protect against malicious or misbehaving code in critical applications. These options are tightly coupled to each processor core to provide redundancy and further reduce single points of failure in the SoC. The cores in an ARC EM Safety Island can also operate in an independent dual-core mode to provide additional performance in applications that do not require lockstep execution, such as those targeting ASIL B safety standards.

The DesignWare ARC MetaWare Development Toolkit for Safety enables developers to generate and debug highly efficient code for deeply embedded applications with an optimizing compiler, debugger and instruction set simulator. The MetaWare compiler toolchain is ASIL D Ready certified and includes a safety manual and a safety guide to help developers meet the requirements of the ISO 26262 standard and prepare for compliance testing of their safety-critical systems. The ARC EM

Safety Islands have been fully validated with fault injection testing using Synopsys' functional safety verification tools, including Certitude® qualification and VCS® simulation, reducing verification time and effort. Verification also includes random fault coverage to ISO 26262 ASIL D levels.

"Advancements in connected vehicles are requiring automotive designers to incorporate sophisticated processor solutions that not only address performance and power, but also safety," said John Koeter, vice president of marketing for IP at Synopsys. "Synopsys' new ASIL D Ready certified ARC EM Safety Islands integrate specific hardware safety features to help designers meet the most stringent ISO 26262 requirements and accelerate development of their automotive SoCs."

Availability & Resources

The ARC EM4SI and EM5DSI Safety Islands and the MetaWare Development Toolkit for Safety are available now. The ARC EM6SI and EM7DSI Safety Islands will be available in Q2, 2017.

Learn more about DesignWare ARC Processor Solutions for Automotive Applications:

- ARC EM Safety Island IP
- Safety Option for ARC EM Processors

Synopsys provides a broad portfolio of IP that is ISO 26262 ASIL B/D Ready certified, AEC-Q100 tested and compliant to the TS 16949 quality management specification. For more information, visit: www.synopsys.com/ip-automotive

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit https://www.synopsys.com/designware.

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About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected release and benefits of the ARC EM6SI and EM7DSI Safety Island processors. Any statements that are not statements of historical fact may be deemed to be forward-looking statements. These statements involve known and unknown risks, uncertainties and other factors that could cause actual results, time frames or achievements to differ materially from those expressed or implied in the forward-looking statements. Other risks and uncertainties that may apply are set forth in the "Risk Factors" section of Synopsys' most recently filed Annual Report on Form 10-K. Synopsys undertakes no obligation to update publicly any forward-looking statements, or to update the reasons actual results could differ materially from those anticipated in these forward-looking statements, even if new information becomes available in the future.

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