Synopsys Extends Verification FastForward Program, Enabling Cadence Incisive and Mentor Graphics Questa Users to Adopt VCS Simulation with Fine-Grained Parallelism Technology

Cheetah Fine-Grained Parallelism Technology Natively Available in VCS 2017.03; Delivers Breakthrough Performance on Existing x86 CPU Server Configurations

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Highlights:

- Synopsys' Verification FastForward Program enables Cadence Incisive and Mentor Graphics Questa users to achieve higher simulation performance by migrating to VCS 2017.03 with native fine-grained parallelism (FGP) on existing x86 CPU server configurations
- Existing VCS users get these additional performance benefits for RTL and gate-level designs with no change to the simulation environment
- Intelligent FGP algorithms deliver performance with minimal impact on simulation compile time and memory
- VCS FGP supports all advanced simulation technologies including Native Low Power (NLP), X-Propagation, and Verdi debug with parallel fast signal database (FSDB)

Synopsys, Inc. (Nasdaq: SNPS) today announced it has extended its Verification FastForward Program to the latest 2017.03 release of its industry-leading, high-performance VCS® functional verification solution. The program enables the users of Cadence® Incisive® and Mentor Graphics® Questa® tools to quickly migrate to VCS 2017.03. This latest VCS release delivers significant simulation performance gains for large SoC designs using native FGP and additional engine optimizations for existing x86 CPU server configurations.

In March 2016, Synopsys announced the patented VCS Cheetah technology that enables FGP in simulation by utilizing many-core CPU architectures. With VCS 2017.03, this breakthrough technology as well as additional performance optimizations, have been integrated and are native to the simulation engines; therefore, no changes or disruption to the existing simulation flows are required. The performance gains can be achieved on existing x86 CPU server platforms and further optimized for user-specific hardware configurations. All existing VCS features such as NLP, X-Propagation simulation, and Verdi® debug with parallel FSDB continue to work as before with no changes necessary to the design or testbenches. Furthermore, intelligent native FGP in VCS delivers the performance boost with minimal impact on compile time and memory usage.

Synopsys is hosting a webinar on February 21, 2017, to provide further technical details on VCS 2017.03 performance innovations, including the native fine-grained parallelism technology and its highly practical use model. Registration for this webinar is available at www.synopsys.com/VCS-FGP.

"The VCS functional verification solution has led the industry in simulation performance for more than 20 years," said Manoj Gandhi, executive vice president and general manager of the Verification Group at Synopsys. "We are excited to once again deliver the next wave of simulation performance natively in VCS. We look forward to continued R&D collaborations with industry leaders to drive innovation in our Verification Continuum Platform."

Availability

General availability of VCS 2017.03 is planned in March 2017. Cadence Incisive and Mentor Questa users interested in joining the FastForward Program should contact their Synopsys representatives.

The Verification FastForward Program

The Verification FastForward Program includes technical services, training and expert verification support. Established in 2011, the program has enabled numerous verification teams to migrate to the VCS solution and has significantly improved their verification performance, effectiveness and productivity. These teams span market segments, company sizes, and geographies and are working on diverse design sizes, verification methodologies and technology nodes.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long

history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected release and benefits of the 2017.03 release of the VCS functional verification solution. Any statements that are not statements of historical fact may be deemed to be forward-looking statements. These statements involve known and unknown risks, uncertainties and other factors that could cause actual results, time frames or achievements to differ materially from those expressed or implied in the forward-looking statements. Other risks and uncertainties that may apply are set forth in the "Risk Factors" section of Synopsys' most recently filed Annual Report on Form 10-K. Synopsys undertakes no obligation to update publicly any forward-looking statements, or to update the reasons actual results could differ materially from those anticipated in these forward-looking statements, even if new information becomes available in the future.

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