Synopsys Takes Hierarchical Timing Signoff Mainstream

New Automation Technology Brings 5x - 10x Reduction in Compute Costs and Runtime

MOUNTAIN VIEW, Calif., Dec. 7, 2016 /PRNewswire/ -- **Highlights:**

- Hierarchical timing reuse reduces schedule-risk while using fewer compute resources
- Automated distribution of full-chip analysis runs on smaller, more readily available resources
- Dynamic top-down and bottom-up block context information enables more accurate signoff

Synopsys, Inc. (Nasdaq: SNPS) today announced 2nd generation technology that enables semiconductor design teams to adopt a smarter, more efficient hierarchical approach to static timing analysis (STA) for timing closure and signoff across all design sizes and levels of complexity. Built on proven PrimeTime® HyperScale hierarchical STA technology and included in the 2016.12 release of the PrimeTime static timing analysis tool, this new capability automates partitioning and distribution of full-chip analysis across a company's private compute cloud, reducing costs and time.

"When we brought the first generation PrimeTime HyperScale technology to our early adopters, it revolutionized the way design teams completed timing closure and signoff on the largest and most complex chips," said Robert Hoogenstryd, senior director of marketing for design analysis and signoff tools at Synopsys. "Our second generation provides additional automation and flexibility, allowing more design teams the opportunity to adopt smarter hierarchical signoff flows while maintaining the gold standard accuracy they expect from PrimeTime."

Flexible Methodology with Proven Hierarchical Technology
HyperScale has been used for static timing analysis on more than 40 of the largest and most complex designs at more than 15 different companies over the last 5 years. These tapeouts include complex graphics, high-performance computing, low-power mobile, and reliable automotive designs.

The 2nd generation of PrimeTime HyperScale technology allows users to easily migrate from flat design analysis to hierarchical block-level analysis and full-chip distributed timing analysis, using mainstream compute resources available in private computing clouds. The hierarchical methodology supports both top-down and bottom-up flows, with state-of-the-art, timing-accurate context generation. This enables HyperScale block-level model analysis to be re-used throughout the flow, instead of re-analyzing the same blocks over and over at each level. The 5x – 10x performance and memory improvements reduce both compute resource cost and schedule risk, for current and future designs.

Market-leading companies who have deployed HyperScale for use in their signoff and tapeout flows include Broadcom Limited, Juniper Networks, MediaTek, Renesas Electronics Corporation, and Samsung Electronics Company.

Availability and Resources
The HyperScale 2nd generation technology is available now as part of the PrimeTime 2016.12 release. For additional information, visit the Synopsys PrimeTime Technology page or contact your local Synopsys account team.

About Synopsys
Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and

semiconductor IP and is also growing its leadership in software quality and security solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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