# Synopsys Advances Test and Yield Analysis Solution for 7-nm Process Node

Increases Test Quality by Targeting Subtle Defects in FinFETs and Emerging Processes

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**Highlights:**

- Innovative slack-based cell-aware test for 7-nm designs increases defect coverage
- FinFET SRAM defect modeling and test algorithms enable efficient test and repair of 7-nm memories
- New diagnostics and yield analysis support for 7-nm reduce turnaround time

Synopsys, Inc. (Nasdaq: SNPS) today announced it expanded its test and yield analysis solution targeting FinFET-specific defects to enable higher quality testing, repair, diagnostics and yield analysis of advanced 7-nanometer (nm) SoCs. To improve defect coverage, Synopsys has been collaborating with several semiconductor companies to advance testing and diagnostics methods for logic, memory and high-speed mixed-signal circuits targeted for manufacture with 7-nm processes. These collaborations are enabling rapid deployment of new functionality within Synopsys' synthesis-based test solution, featuring TetraMAX® II ATPG, DesignWare® STAR Memory System®, and DesignWare STAR Hierarchical System.

Leading semiconductor companies ramping up design capabilities for emerging 7-nm processes are facing increasing test quality and yield management challenges. To address these challenges, Synopsys' test solution delivers several innovative technologies that target defects occurring more frequently at emerging process nodes. For logic circuits, new modeling techniques, such as resistance sweeping, improve the ability of slack-based cell-aware tests to detect defects such as intra-cell partial bridges that are more prevalent with advanced FinFET processes. For embedded memory test and repair, the STAR Memory System solution incorporates custom algorithms based on silicon learning at the industry's top silicon foundries to detect and repair defects exemplified by resistive fin shorts, fin opens and gate-fin shorts. Furthermore, the DesignWare STAR Hierarchical System enables high coverage manufacturing and characterization test patterns for the 7-nm DesignWare PHY IP to be efficiently applied through the SoC hierarchy.

To accelerate diagnosis of 7-nm yield issues, defect isolation to specific areas within design cells is possible through new support of cell-aware descriptions in the database shared between TetraMAX II ATPG and Yield Explorer® solutions. The combination of test and diagnostic advances increase 7-nm defect detection and speed up failure analysis and yield ramp in production manufacturing environments.

"The growing complexity and process variation found with advanced 7-nm FinFET processes requires improved test and yield technologies," said John Koeter, vice president of marketing for IP and prototyping at Synopsys. "Our IP design teams are leveraging TetraMAX ATPG as well as STAR Memory System and STAR Hierarchical System test, repair and diagnostic solutions to help multiple customers designing with 7-nm IP improve their product quality and yield, while accelerating their time to market."

"As a leading provider of comprehensive test and yield solutions, Synopsys is committed to helping designers meet their growing challenges of higher quality and faster yield ramp," said Bijan Kiani, vice president of product marketing for the Design Group at Synopsys. "Through our on-going collaborations with leading semiconductor companies worldwide, we are delivering innovative solutions to address the specific requirements for advanced FinFET processes. These innovations will enable our customers to rapidly adopt 7-nm technologies to meet their goals for high-performance SoC products."

**About the Synopsys Synthesis-Based Test Solution**

The Synopsys synthesis-based test solution comprises DFTMAX™ Ultra, DFTMAX, and TetraMAX I and II for power-aware logic test and physical diagnostics; DFTMAX LogicBIST for in-system self-test; SpyGlass® DFT ADV for testability analysis; the DesignWare STAR Hierarchical System for automated hierarchical testing of IP and logic blocks on an SoC; DesignWare STAR Memory System for embedded test, repair and diagnostics; the Z01X™ fault simulator; Yield Explorer design-centric yield analysis; and the Camelot™ software system for CAD navigation. Synopsys' test solution combines Design Compiler® RTL synthesis with embedded test technology to optimize timing, power, area and congestion for test as well as functional logic, leading to faster time-to-results. The Synopsys test solution delivers tight integration across the Synopsys Galaxy™ Design Platform, including Design Compiler synthesis, IC Compiler™ II place and route, and PrimeTime® timing analysis, to enable faster turnaround time while meeting both design and test goals, higher defect coverage and faster yield ramp.

## About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software security and quality solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest security and quality, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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