# Synopsys' Galaxy Design Platform Enables Superior Low-Power Designs on Samsung's 10-nm Process Technology

Platform Certified for Samsung's Second Generation of 10nm Process (10LPP)

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**Highlights:**

- 64-bit ARM Cortex-A53 processor used for QoR optimization and flow validation for Samsung's 10LPP process
- Power reduction delivered through several technologies in Design Compiler Graphical and IC Compiler II, including multibit registers and low-power placement technologies
- Certification includes scalable reference flow based on Lynx Design System

Synopsys, Inc. (Nasdaq: SNPS) today announced that Samsung Electronics Co., Ltd. has certified the Synopsys Galaxy™ Design Platform for Samsung's second generation of 10nm LPP (Low Power Plus) process. The 10LPP process delivers high performance for compute-intensive designs and lower power consumption for various applications. Galaxy certification for Samsung's10LPP process includes design techniques for enabling less power consumption such as multibit register optimization, low-power placement, and In-Design rail and power analysis, all of which have been deployed on production designs at Samsung's 10LPP process. Synopsys' SiliconSmart® library characterization tool was used to develop the foundation IP used for this certification process and reference flow. This certification also includes a reference flow, compatible with Synopsys' Lynx Design System, which includes scripts for automation and design best practices.

"Built through deep collaboration with Synopsys, this elaborate certification and reference flow for our 10LPP process will let our mutual customers achieve the best power and performance for their designs," said Jaehong Park, senior vice president of Design Service Team at Samsung Electronics. "Our foundry customers can confidently ramp their designs to volume production on our most advanced FinFET-based process using the proven Galaxy Design Platform."

"Our tools and reference flow collaboration with Samsung is focused on enabling designers to get the optimum QoR with highest confidence on Samsung's latest 10LPP process," said Bijan Kiani, vice president of product marketing for Synopsys' Design Group. "This exclusive scalable reference flow will allow designers to easily achieve their desired performance and power targets."

Key Synopsys tools and features of this Galaxy Design Platform reference flow, certified using the ARM® Cortex®-A53 processor, include:

- Design Compiler® Graphical RTL synthesis: Correlation, congestion reduction, multibit register optimization, low-power placement and physical guidance for IC Compiler™ II place-and-route system
- DFTMAX™ and TetraMAX® II test: FinFET-based, cell-aware and slack-based transition testing for higher test quality
- Formality® formal verification: UPF-based equivalence checking with state transition verification
- IC Compiler II place and route: Multi-pattern and color-aware physical implementation with multibit register optimization, low-power placement and advanced design planning for optimized module placement and timing
- IC Validator signoff physical verification: In-Design, automated DRC repair, DFM pattern matching and DFM metal fill within IC Compiler II place-and-route system; and LVS signoff
- PrimeTime® timing signoff: Ultra-low voltage timing signoff with Advanced Waveform Propagation (AWP), Parametric On-Chip Variation (POCV) analysis and placement rule-aware Engineering Change Order (ECO) guidance
- StarRC™ extraction: Multi-patterning, full color-aware variation and 3D FinFET modeling
- PrimeRail reliability analysis: In-Design static and dynamic analysis for electromigration and IR-drop integrity

The reference flow of 10LPP process is compatible with Synopsys' Lynx Design System, a full-chip design environment that includes innovative automation and reporting capabilities to help designers implement and monitor their designs. It includes a production RTL-to-GDSII flow that simplifies and automates many critical implementation and validation tasks, enabling engineers to focus on achieving performance and design goals.

To learn more, attend the joint Samsung and Synopsys session on using the 10nm reference flow for tapeout success at the ARM TechCon Conference (October 26, 2016 at the Santa Clara Convention Center).

**About Synopsys**

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP, and is also growing its leadership in software quality and security solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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