TSMC and Synopsys Collaboration Delivers Innovative Technologies for the High Performance Compute (HPC) Platform

Scope of Collaboration Includes Innovations in Place-and-Route Optimization Technologies for High-Performance Designs

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Highlights:

- Innovations include multiple new implementation technologies including via pillar and clock tree optimizations in IC Compiler II
- Both companies initiate Design Compiler Graphical synthesis collaboration for high performance compute designs
- Synopsys will deliver a specially created flow to enable designers to maximize performance from the TSMC HPC Platform
- Collaboration will produce industry-first ASIC-based flow and methodology with several new technologies to enable high-performance, compute-intensive designs

Synopsys, Inc. (Nasdaq: SNPS) today announced its collaboration with TSMC to deliver innovative technologies to enable adoption of TSMC's High Performance Compute (HPC) Platform. The new technologies, enabled through TSMC and Synopsys collaboration, will be available in the Synopsys' Galaxy™ Design Platform for the 7-nanometer (nm) process in November 2016. Via pillar, multi-source clock tree synthesis (CTS) with hybrid clock mesh and automated bus routing to match resistance and capacitance on critical nets are some examples of the jointly developed technologies. With these innovations, TSMC and Synopsys will enable designers to create cutting-edge, high-performance designs at the 7-nm process node.

Via pillar is a new technology that aims to reduce via resistance and increase electromigration robustness for enhanced performance. Via pillar is supported in IC Compiler™ II place and route system, and is enabled for what-if analysis in Design Compiler Graphical®. This includes insertion of via pillars in the netlist, modeling of via pillars in virtual route, legalized placement of via pillars, as well as detailed routing, extraction and timing to support via pillars. The multi-source CTS with hybrid clock mesh in IC Compiler II inserts via pillars on clock nets, and then the global and detailed routers adjust the signal routes to insert the via pillars. IC Compiler II provides low skew, high-performance clock designs with highly customizable mesh and automatic H-tree creation for clocks. IC Compiler II also provides automated bus routing to match resistance and capacitance on critical nets. It supports non-default routing and user-specified layer width and spacing.

"Synopsys' expertise in delivering an integrated flow from front-end to physical implementation, combined with TSMC's leadership in process technology, makes delivery of innovations that enable high-performance designs possible," said Bijan Kiani, vice president of product marketing for the Design Group at Synopsys. "These innovations will enable our mutual customers to build some of the most advanced, high-performance designs today."

"We want to ensure that semiconductor designers are able to build the fastest chips using the latest process technology to meet the high-performance needs of modern SoCs," said Suk Lee, TSMC senior director, Design Infrastructure Marketing Division. "In the current design flow, full custom or semi-custom flows and methodology are used to achieve higher speed. Through our collaboration with Synopsys, we are enabling a new ASIC-based design flow and methodology for our High Performance Compute Platform."

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP, and is also growing its leadership in software quality and security solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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