Synopsys and TSMC Collaborate on Development of Interface and Foundation IP for 7-nm FinFET Process

Joint Efforts Result in Multiple 7-nm Customer Tapeouts of DesignWare Logic Libraries and Embedded Memories

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Highlights:

- Successful customer tapeouts of Synopsys DesignWare Logic Libraries and Embedded Memories on 7-nm demonstrates high quality and reduces integration risk
- Integrated Synopsys STAR Memory System solution enables efficient test and repair of 7-nm memories
- Early development of IP enables first wave of 7-nm designs targeting mobile and high-performance computing applications
- DesignWare Interface IP in development for TSMC 7-nm process includes USB, PCI Express, DDR, MIPI, DisplayPort, SATA and Ethernet

Synopsys, Inc. (Nasdaq: SNPS) today announced the successful tapeout of multiple customer test chips with DesignWare® Logic Libraries and Embedded Memories for TSMC's 7-nanometer (nm) FinFET process. The tapeouts mark a significant milestone in Synopsys' and TSMC's collaboration on the development of DesignWare Logic Library, Embedded Memory and Interface IP for TSMC's 7-nm FinFET process. The collaboration extends Synopsys' long history of successful IP development on TSMC advanced FinFET processes for high-performance, low-power system-on-chips (SoCs).

"TSMC and Synopsys have a long track record of successful collaboration on advanced FinFET processes, providing our mutual customers with a low-risk path to integrating a broad portfolio of high-quality, silicon-proven IP into their SoCs," said Suk Lee, TSMC senior director, Design Infrastructure Marketing Division. "Achieving multiple customer tapeouts of Synopsys DesignWare IP on TSMC's 7-nm process demonstrates the benefits of our collaboration and gives designers confidence that they will meet their power, performance and area targets while accelerating their time to market."

"As a leading provider of physical IP, Synopsys continues to provide early access to IP in the most advanced process technologies, helping designers incorporate necessary functionality and accelerate their design schedules," said John Koeter, vice president of marketing for IP and prototyping at Synopsys. "With multiple customer tapeouts of DesignWare IP for TSMC's 7-nm process, Synopsys enables designers to reduce integration risk and differentiate their products with this latest technology."

Availability

DesignWare Logic Libraries and Embedded Memories for the TSMC 7-nm process are available now. The STAR Memory System® is also available now for all TSMC process technologies.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software quality and security solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at http://www.synopsys.com/.

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