Synopsys Introduces ARC Security Processors for Low-Power Embedded Applications

DesignWare ARC SEM Security Processors with SecureShield Technology Protect Against Side-Channel Attacks, IP Theft and Data Breaches

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Highlights:

- New ultra-low power ARC SEM processors incorporate advanced security features to protect systems from evolving threats
- Timing and power randomization features protect against side-channel attacks on high-value targets such as smart metering, NFC payment and embedded SIM applications
- Cryptographic functions are performed in a secure software environment versus dedicated hardware, reducing silicon area
- Enhanced memory protection unit and SecureShield Runtime Library simplify development of a Trusted Execution Environment

Synopsys, Inc. (Nasdaq:SNPS) today announced availability of the DesignWare® ARC® SEM110 and SEM120D security processors for low-power, embedded applications such as smart metering, NFC payment and embedded SIMs. The new ARC SEM processors with Synopsys SecureShield™ technology enable designers to protect systems against software, hardware and side-channel attacks as well as separate secure and non-secure functions as part of a Trusted Execution Environment (TEE). The ultra-low power, performance-efficient ARC SEM processors offer advanced security features such as uniform instruction timing and power randomization to obfuscate secure operations. In addition, the SecureShield Runtime Library manages the partitioning and isolation of containers within a TEE to ensure data is stored and processed in a safe environment. This combination of hardware and software features enables designers to create more secure system-on-chips (SoCs) for IoT and mobile applications.

ARC SEM Security Processors

The DesignWare ARC SEM Processors are based on the scalable, 32-bit ARCv2 instruction set architecture (ISA) and are optimized for area and power efficiency. The ARC SEM110 Processor integrates a wide range of security technologies and can be implemented in an SoC as either a standalone secure core or as a single core performing both secure and non-secure functions. The ARC SEM120D adds DSP functionality for applications such as sensor processing and voice identification in health care and IoT devices. Key features of the new processors include:

- Side-channel resistance with uniform instruction timing and timing/power randomization obfuscate secure operations from potential hackers
- An enhanced memory protection unit and SecureShield technology simplify development of a TEE
- Tamper-resistant pipeline with in-line instruction/data encryption and address scrambling, and data integrity checks protect against system attacks and IP theft
- Integrated watchdog timer detects system failures including tampering
- DSP instructions and unified MUL/MAC unit in the ARC SEM120D support applications requiring enhanced security and real-time processing

"High-profile security breaches are increasingly in global headlines, underscoring the need to ensure the right precautions are being taken during SoC design and test," said Mats Nählinder, president of Riscure North America. "As a global security test lab and a market leader in side-channel test equipment, our business is to evaluate security solutions for their ability to protect against such malicious attacks targeting hardware and software. The DesignWare ARC SEM processors enable designers to add protection to their embedded devices against such attacks."

ARC Software, Development Tools and Ecosystem

Synopsys' embARC Open Software Platform provides software developers with online access to a comprehensive suite of free and open-source software, including security transport protocols. The platform includes the new SecureShield Runtime Library, which runs in the background and manages the partitioning and isolation of containers within a TEE.

Like all ARC processors, the ARC SEM processors are supported by a robust ecosystem of software and

hardware development tools, including:

- MetaWare Development Toolkit that generates highly efficient code ideal for deeply embedded applications
- ARC nSIM fast instruction set simulator enables early software development
- ARC xCAM provides 100 percent cycle-accurate simulation for software optimization and system verification

In addition, support for Synopsys' HAPS® physical prototyping system enables early software development, hardware/software integration and system validation of ARC SEM processor-based designs.

The ARC SEM processors with SecureShield are part of Synopsys' comprehensive portfolio of security IP solutions that include the Enhanced Security Package and CryptoPack options for ARC EM processors and the DesignWare Security IP solutions, which consist of a range of cryptography cores and software library, protocol accelerators, root of trust, platform security and content protection IP.

"As security threats become more prevalent in connected devices, having security built-in at the SoC level is critical to minimizing the risk of side-channel attacks, data breaches, IP theft and more," said John Koeter, vice president of marketing for IP and prototyping at Synopsys. "By expanding our portfolio of IP solutions with the new ARC SEM processors, Synopsys enables designers to integrate the necessary security features into their embedded devices, while meeting the stringent power and area requirements of their chips."

Availability and Resources

The DesignWare ARC SEM110 and SEM120D processors are scheduled for general availability in October 2016.

- Learn more about the ARC SEM Processors: https://www.synopsys.com/dw/ipdir.php?ds=arc-sem
- Learn more about ARC SecureShield Technology: http://www.secureshield.com/
- Learn more about Synopsys' DesignWare Security IP Solutions: http://www.synopsys.com/IP/security-ip/Pages/default.aspx

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software quality and security solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected release and benefits of the DesignWare ARC SEM110 and SEM120D processors. Any statements that are not statements of historical fact may be deemed to be forward-looking statements. These statements involve known and unknown risks, uncertainties and other factors that could cause actual results, time frames or achievements to differ materially from those expressed or implied in the forward-looking statements. Other risks and uncertainties that may apply are set forth in the "Risk Factors" section of Synopsys' most recently filed Quarterly Report on Form 10-Q. Synopsys undertakes no obligation to update publicly any forward-looking statements, or to update the reasons actual results could differ materially from those anticipated in these forward-looking statements, even if new information becomes available in the future.

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