Toshiba Plans Deployment of Synopsys TetraMAX II on Upcoming SoC Design

New ATPG Solution Reduces Pattern Count by up to 50% and Significantly Shortens ATPG Runtime

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Highlights:

- Thorough evaluation of TetraMAX II demonstrated significant reductions in both pattern count and runtime without impacting test coverage
- TetraMAX II was up and running in Toshiba's flow with minimal effort
- Toshiba is planning to deploy TetraMAX II and its advanced power-aware ATPG capabilities on their upcoming SoC design.

Synopsys, Inc. (Nasdaq: SNPS), today announced that Toshiba has confirmed that Synopsys TetraMAX® II ATPG can significantly accelerate test pattern generation and reduce manufacturing test time and cost. Required to meet aggressive test quality and design schedule goals on an upcoming complex SoC, Toshiba designers determined they would need a much faster ATPG solution that generates much fewer test patterns while being fully power-aware. To address these needs, and following a thorough evaluation demonstrating up to 50% reduction in pattern count, significantly faster runtime and advanced power-aware features, Toshiba is planning to deploy TetraMAX II for their latest consumer electronics SoC design. Toshiba will be sharing their experience with TetraMAX II at the Synopsys Users Group (SNUG) India conference, opening July 13th at the Leela Palace Hotel in Bangalore.

"Long ATPG runtimes and increasing test pattern counts are becoming bigger challenges on our large-scale SoC designs. Test pattern reduction within a short runtime is required to minimize test cost while maintaining the quality of test." said Kazunari Horikawa, senior manager at Toshiba's Design Technology Development Dept. "We have been collaborating with Synopsys, and confirmed through an evaluation that TetraMAX II shortens ATPG execution time and reduces the number of test patterns by up to 50% while maintaining the quality of test. We are planning to adopt TetraMAX II for our upcoming SoC designs and believe TetraMAX II will further reduce test cost with its strong roadmap."

"Synopsys is committed to addressing the evolving test requirements for designers worldwide " said Antun Domic, executive vice president and general manager for Synopsys' Design Group. "Our recent collaboration with Toshiba demonstrates our continuous innovation and investment in new test technologies that addresses our customers' need for shorter manufacturing test time and faster ATPG while their designs complexity continues to grow."

About TetraMAX II

TetraMAX II is built on new test generation, fault simulation and diagnosis engines that are extremely fast, exceedingly memory efficient, highly optimized for generating patterns and execute fine-grained multithreading of the ATPG and diagnosis processes. These innovations lead to significantly fewer test patterns and cut ATPG time from days to hours. The memory efficiency of TetraMAX II enables utilization of all server cores regardless of design size surpassing previous solutions that are limited by high memory usage. The reuse of production proven design modeling and rule checking infrastructure, as well as user and tool interfaces, ensure designers can quickly deploy TetraMAX II risk-free on their most challenging designs. Moreover, TetraMAX II utilizes established links with the Galaxy™ Design Platform tools, such as DFTMAX™ compression, PrimeTime® timing analysis and StarRC™ extraction, as well as other Synopsys tools including Yield Explorer® design-centric yield analysis and Verdi® debug tools, to deliver the highest quality test and the fastest, most productive flows.

About the Synopsys Synthesis-Based Test Solution

The Synopsys synthesis-based test solution is comprised of DFTMAX Ultra, DFTMAX and TetraMAX I and II for power-aware logic test and physical diagnostics; DFTMAX LogicBIST for in-system self-test; SpyGlass® DFT ADV for testability analysis; the DesignWare® STAR Hierarchical System for hierarchical test of IP and cores on an SoC; the DesignWare STAR Memory System® for embedded test, repair and diagnostics; the Z01X™ fault simulator; Yield Explorer® for design-centric yield analysis; and the Camelot™ software system for CAD navigation. Synopsys' test solution combines Design Compiler® RTL synthesis with embedded test technology to optimize timing, power, area and congestion for test as well as functional logic, leading to faster time-to-results. The Synopsys test solution delivers tight integration across the Synopsys Galaxy Design Platform, including Design Compiler, IC Compiler™ II place and route, and PrimeTime timing analysis, to enable faster

turnaround time while meeting both design and test goals, higher defect coverage and faster yield ramp.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP, and is also growing its leadership in software quality and security solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Editorial Contact:
Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

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