TetraMAX II Shortens Test Pattern Generation From Days to Hours

New ATPG Engines Reduce Test Cost, Pattern Count by 25 Percent with Order of Magnitude Faster Runtime

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Highlights:

- Order of magnitude faster ATPG ensures on-time availability of patterns for testing first silicon samples
- Significant pattern reduction enables designers to reduce test cost or alternatively increase test quality at the same cost per design requirements
- Re-use of proven interfaces enables risk-free, easy deployment

Synopsys, Inc. (Nasdaq: SNPS), today announced its next-generation ATPG and diagnostics solution, TetraMAX® II, incorporating the innovative test engines unveiled at the International Test Conference in October 2015. Delivering an order of magnitude faster runtime, TetraMAX II cuts ATPG runtime from days to hours, ensuring patterns are ready when early silicon samples are first available for testing. Additionally, TetraMAX II generates 25 percent fewer patterns, allowing IC design teams to shorten the time and lower the cost of testing silicon parts or, if required by specific market segments such as automotive, increase the quality of test without impacting test cost. Reuse of production-proven ATPG interfaces ensures risk-free, easy deployment into design and test flows. Users will share their experience with TetraMAX II at the Synopsys Users Group (SNUG) India conference at the Leela Palace Hotel inBangalore.

TetraMAX II is built on new test generation, fault simulation and diagnosis engines that are extremely fast, exceedingly memory efficient, highly optimized for generating patterns and capable of executing fine-grained multithreading of the ATPG and diagnosis processes. These innovations lead to significantly fewer test patterns and cut ATPG time from days to hours. Unparalleled memory efficiency of TetraMAX II enables utilization of all server cores regardless of design size, surpassing previous solutions that are limited by high memory usage. The reuse of production proven design modeling and rule checking infrastructure, as well as user and tool interfaces, ensures designers can quickly deploy TetraMAX II risk-free on their most challenging designs. Moreover, TetraMAX II utilizes established links with Synopsys Galaxy Design Platform tools, such as DFTMAX ™ solution, PrimeTime® timing analysis and StarRC extraction tool, and other Synopsys tools, including Yield Explorer® yield management and Verdi® debug tools, to deliver the highest quality test and the fastest, most productive flows.

"Designers worldwide rely on Synopsys' synthesis-based test solution to achieve the highest test quality on their most challenging designs," said Antun Domic, executive vice president and general manager for Synopsys' Design Group. "TetraMAX II demonstrates our commitment to continually deliver innovative and groundbreaking test technologies and addresses our customers need for faster ATPG and diagnostics as well as reduced silicon test time."

About the Synopsys Synthesis-Based Test Solution
The Synopsys synthesis-based test solution is comprised of SpyGlass® DFT ADV testability analysis, DFTMAX, DFTMAX Ultra, TetraMAX I and II for power-aware logic test and silicon diagnostics; the DesignWare® STAR Hierarchical System for hierarchical test of IP and cores on an SoC; the DesignWare STAR Memory System® solution for embedded test, repair and diagnostics; the Yield Explorer tool for design-centric yield analysis; and the Camelot™ software system for CAD navigation. Synopsys' test solution combines Design Compiler® RTL synthesis solution with embedded test technology to optimize timing, power, area and congestion for test as well as functional logic, leading to faster time-to-results. The Synopsys test solution delivers tight integration across the Synopsys Galaxy Design Platform, including Design Compiler, IC Compiler™ II place and route tool, and PrimeTime® timing signoff, to enable faster turnaround time while meeting both design and test goals, higher defect coverage and faster yield ramp.

About Synopsys
Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP, and is also growing its leadership in software quality and security solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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