Synopsys TetraMAX II Speeds Test Generation for STMicroelectronics SoC Designs

New ATPG Engines Substantially Reduce Test Pattern Count for Lower Test Cost

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Highlights:

- Evaluation of TetraMAX II demonstrated an order of magnitude speedup in runtime
- Achieves significant test-pattern-count reduction without impacting test coverage

Synopsys, Inc. (Nasdaq: SNPS), today announced that STMicroelectronics is seeing significantly faster test pattern generation runtime and reduced number of patterns with TetraMAX® II ATPG. STMicroelectronics faces the challenges of increasing complexity and shrinking time-to-market schedules for their system-on-chip (SoC) designs. To meet these challenges, STMicroelectronics requires fast turn-around time (TAT) for generating high-quality manufacturing test patterns. Following an evaluation using a multi-million-gate FD-SOI SoC design, TetraMAX II demonstrated an order of magnitude speedup in runtime and significant test-pattern-count reduction without impacting test coverage. As a result, STMicroelectronics is deploying TetraMAX II in their standard SoC design flow.

"Over the past several years, we have collaborated with Synopsys to address the growing manufacturing-test challenges of increasing complexity and manufacturing test costs in combination with requirements for higher quality and faster TAT," said Roberto Mattiuzzo, SoC integration and DFT methodologies manager in STMicroelectronics' Digital and Mixed Processes ASIC division. "During our evaluation on a high-density FD-SOI chip, TetraMAX II produced test patterns an order of magnitude faster while significantly reducing the number of patterns without any coverage loss. With these results, we are confidently testing first-silicon samples earlier and reducing tester time, too."

"Customers such as STMicroelectronics rely on Synopsys' test solution to ensure the best combination of fast TAT and low test costs with high quality," said Antun Domic, executive vice president and general manager for Synopsys' Design Group. "Our long-term collaboration with ST continues to go from strength to strength. With the latest results from their TetraMAX II evaluation, we are demonstrating yet again our commitment to deliver continuous innovations in ATPG and related technologies to address our customers' manufacturing test challenges."

About TetraMAX II
TetraMAX II is built on new test generation, fault simulation and diagnosis engines that are extremely fast, exceedingly memory efficient, highly optimized for generating patterns and execute fine-grained multithreading of the ATPG and diagnosis processes. These innovations lead to significantly fewer test patterns and cut ATPG time from days to hours. The memory efficiency of TetraMAX II enables utilization of all server cores regardless of design size surpassing previous solutions that are limited by high memory usage. The reuse of production proven design modeling and rule checking infrastructure, as well as user and tool interfaces, ensure designers can quickly deploy TetraMAX II risk-free on their most challenging designs. Moreover, TetraMAX II utilizes established links with the Galaxy™ Design Platform tools, such as DFTMAX compression, PrimeTime® timing analysis and StarRC™ extraction, as well as other Synopsys tools, including Yield Explorer® design-centric yield analysis and Verdi® debug tools, to deliver the highest quality test and the fastest, most productive flows.

About the Synopsys Synthesis-Based Test Solution

The Synopsys synthesis-based test solution is comprised of DFTMAX Ultra, DFTMAX and TetraMAX I and II for power-aware logic test and physical diagnostics; DFTMAX LogicBIST for in-system self-test; SpyGlass® DFT ADV for testability analysis; the DesignWare® STAR Hierarchical System for hierarchical test of IP and cores on an SoC; the DesignWare STAR Memory System® for embedded test, repair and diagnostics; the Z01X™ fault simulator; Yield Explorer® for design-centric yield analysis; and the Camelot™ software system for CAD navigation. Synopsys' test solution combines Design Compiler® RTL synthesis with embedded test technology to optimize timing, power, area and congestion for test as well as functional logic, lead to faster time-to-results. The Synopsys test solution delivers tight integration across the Synopsys Galaxy Design Platform, including Design Compiler, IC Compiler™ II place and route, and PrimeTime timing analysis, to enable faster turnaround time meeting both design and test goals, higher defect coverage and faster yield ramp.

About Synopsys
Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP, and is also growing its leadership in software quality and security solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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