Synopsys Optimizes DesignWare IP for PCI Express 4.0 Architecture to Reduce Latency by up to 20 Percent

New Enhanced PCI Express IP Supports 16 GT/s and Latest Specification, Targeting High-Performance Applications

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Highlights:

- Synopsys' optimized PHY and Controller IP for PCI Express architecture reduces latency by 20 percent and area by 15 percent
- Lane margining capability assesses system performance for design robustness
- Testing within the ecosystem ensures interoperability and reduces integration risk
- See demonstrations at PCI-SIG DevCon in Santa Clara, CA, June 28-29

Synopsys, Inc. (Nasdaq:SNPS), today announced the immediate availability of its optimized DesignWare® PHY and Controller IP Solution for PCI Express® (PCIe®) 4.0 architecture, which reduces latency by up to 20 percent and area by 15 percent compared to the previous implementation. The PCI Express PHY and Controller IP supports lane margining, allowing system designers to assess performance variation tolerance for design robustness. By supporting the latest PCI Express 4.0 specification, the DesignWare IP solution provides proven interoperability and addresses the stringent performance requirements of cloud computing and automotive applications.

"Synopsys' DesignWare PHY and Controller IP for PCI Express 4.0 technology has been tested for interoperability using the Teledyne LeCroy Summit Z416 Protocol Analyzer/Exerciser, which is targeted to test for PCIe 4.0 compliance in the near future," said John Wiedemeier, product marketing manager at Teledyne LeCroy. "This is an important indicator to all designers and the ecosystem that the DesignWare IP works as expected and meets the latest PCI Express specification requirements, mitigating risk and accelerating time-to-market."

In the transition from the PCI Express 2.0 to PCI Express 3.0 specification, increases in speed, protocol changes and new equalization schemes led to design complexities and silicon issues. To ease the transition to the PCI Express 4.0 architecture, to provide more visibility into the performance of the interface, and to help designers to quickly diagnose issues and validate silicon, Synopsys offers extensive error injection and debug capabilities for silicon analysis along with built-in self-test (BIST) and automatic test equipment (ATE) test vectors for a complete at-speed production testing. In addition, designers can utilize Synopsys' available IP Prototyping Kits and IP Virtualizer Development Kits for PCI Express 4.0 technology to accelerate their SoC and software development.

"Our customers are consistently challenged with meeting their design performance and area requirements for advanced data-intensive cloud computing applications," said John Koeter, vice president of marketing for IP and prototyping at Synopsys. "By providing an optimized PCI Express IP solution that significantly reduces latency and area, Synopsys is enabling designers to meet their key design requirements and deliver differentiated products."

Availability and Additional Resources

The complete DesignWare IP Solution for PCI Express technology, supporting transfer speeds from 16 GT/s down to 2.5 GT/s on a range of process nodes from 65-nanometer (nm) to 10-nm FinFET, is available now. The IP Prototyping Kits, Software Development Kits, and verification IP for PCI Express 4.0 technology are also available now.

Hear Synopsys presentations and see the latest DesignWare IP for PCIe demonstrations at PCI-SIG® DevCon in Santa Clara, CA, June 28-29, 2016.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enable designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP, and is also growing its leadership in software quality and security solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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