Synopsys' New Suite of DDR4 IP Features Increases Capacity and Reliability of High-Performance Cloud Computing Systems

DesignWare DDR4 IP Solution Enables Servers to Solve Complex Computation Problems Faster

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Highlights:

- Expands memory capacity by up to 400 percent without degrading performance
- Enables reconstruction of all data in a failed DRAM with advanced error correcting code
- Offers highest design margin and signal integrity with embedded calibration processor
- Reduces system downtime by retrying failed memory commands

Synopsys, Inc. (Nasdaq:SNPS) today announced a suite of new features for its 3200 Mbps DesignWare® DDR4 IP to expand memory capacity for high-performance cloud computing systems while improving reliability, accessibility and serviceability (RAS). The DDR IP supports advanced error correcting code (ECC), which can correct all DRAM failures within a device to enable replacement of defective DIMMs without data loss. In addition, support for high-capacity DDR4 LRDIMM and DDR4 3D Stacked (DDR4-3DS) DRAM with 16 ranks of memory expands capacity by up to 400 percent compared to the previously supported four ranks, without reducing performance. The IP includes the industry's only embedded calibration processor, which can train the system at power-up to improve design margin and signal integrity. The calibration processor can also train up to four active operating modes to manage rapid power and frequency requirement changes. Synopsys' DDR4 Controller and PHY IP solution enables cloud and virtualized server environments to support larger numbers of clients simultaneously and quickly solve complex computation problems.

"As the DRAM requirements for networking, storage and security applications increase, efficient access to more memory is critical," said Matthias Buchner, director of compute and networking marketing at Micron Technology, Inc. "System architects are dramatically improving their products' reliability, capacity and performance with SDRAM DDR4 from Micron. Synopsys' DDR4 IP further expands accessible memory capacity without degrading performance, enabling designers to increase their systems' overall capabilities."

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The DesignWare uMCTL2 Memory Controllers and uPCTL2 Protocol Controllers support DDR4/3 and LPDDR4/3 standards and offer strong RAS features. The controllers' DDR4 command/address (CA) parity and write cyclic redundancy check (CRC) with retry features provide data and command/address integrity, allowing the system to recover from a command or address error by returning to the last known good state and retrying the failed command. New advanced ECC within the controllers uses modified Reed-Solomon coding to correct up to four consecutive data bits in each word, as may be required during a complete failure of one DRAM device connected to a system-on-chip (SoC).

To assist with system-level optimization, the new embedded calibration processor within the DesignWare DDR4/3 PHY facilitates design-for-test (DFT) functionality by generating two-dimensional read and write data eyes for every bit of the bus that can be captured by the IP. Up to four active operating states are trained at boot time and maintained as voltages and temperatures change. Each active operating state can have unique frequencies, equalization settings and termination settings to allow the host SoC to change its operating mode based on the power and frequency requirements.

"Memory access has become an important design consideration in high-performance storage, computing and cloud server applications," said John Koeter, vice president of marketing for IP and prototyping at Synopsys. "By providing differentiated functionality, including support for high-capacity LRDIMM, advanced ECC and embedded calibration, Synopsys enables designers to significantly increase the memory capacity of their systems without sacrificing the maximum operating frequency."

Availability & Resources

The new features for the DesignWare uMCTL2 Memory Controllers, DesignWare uPCTL2 Protocol Controllers and DesignWare DDR4/3 PHYs are available now. In addition to the controllers and PHYs, Synopsys' complete DDR4 IP solution includes IP subsystems, IP prototyping kits, IP software development kits, verification IP, and performance analysis using DesignWare DDR Explorer and Platform Architect MCO.

- Register for the webinar, "DDR4 for Enterprise Applications": https://webinar.techonline.com/1878?

keycode=CAA1GC
- Learn more about DesignWare DDR IP: www.synopsys.com/ddr

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software quality and security solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at http://www.synopsys.com/.

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