Avnet ASIC Israel Ltd. (AAI) Standardizes on Synopsys' Design Compiler Graphical to Accelerate SoC Design Cycle

RTL Congestion Analysis and Tight Correlation to Place-and-Route Shorten Design Schedules and Improve Predictability

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Highlights:

- Avnet ASIC Israel has standardized on Design Compiler Graphical for implementation of SoC designs
- Early RTL congestion analysis and optimization with tight correlation through physical guidance to IC Compiler II cuts two to three weeks off RTL-to-GDSII schedule

Synopsys, Inc. (Nasdaq: SNPS), today announced that Avnet ASIC Israel (AAI), a provider of system-on-chip (SoC) design, layout and manufacturing services, has standardized on Synopsys Design Compiler® Graphical RTL synthesis solution to accelerate the design of their SoCs. Improving design implementation turnaround time (TAT) and predictability are key goals for AAI to deliver competitive, cost-effective COT design services to their customers. To help meet these goals, AAI has deployed a fast turnaround implementation flow that includes early RTL analysis to identify and remove routing congestion with Design Compiler Graphical, followed by physical guidance to IC Compiler™ II place-and-route solution. In addition, AAI uses advanced low power and design-for-test techniques within this flow. As a result, AAI achieves rapid turnaround for their SoC designs, saving an average of two to three weeks in their overall RTL-to-GDSII schedule.

"Improving the RTL-to-GDSII schedule of our COT design services is a critical goal to enable the success of our fabless and system design customers," said Pavel Vilk, engineering director at AAI. "Design Compiler Graphical enables our design team to identify and remove routing congestion early in the flow and, with physical guidance to IC Compiler II, it enables us to speed up the critical physical place-and-route and final design closure phases. Among the many benefits of using Design Compiler Graphical, our engineers like the ability to pinpoint specific RTL source code that causes congestion, especially in our larger blocks of over three million instances, so they can make fixes quickly before moving forward with place-and-route. As a result of our successful deployment experience with typical schedule savings of two to three weeks, we have standardized on Design Compiler Graphical for all our designs and are considering further flow improvements with close collaboration with Synopsys."

A few highlights of the latest release of Design Compiler, 2016.03, include:

- 25 percent faster runtime enabling the synthesis of designs as large as 5 million instances in hours vs. days
- 10 percent reduction in total negative slack (TNS) for faster design closure
- Tighter timing correlation for designs at 16-nanometer and 10-nanometer due to improved local timing delay estimates for complex floorplans, automatic estimation of via resistance based on process technology and layer promotion of up to 15 layers
- Congestion reduction targeted for designs with large sparse multiplexers delivering up to 30 percent area reduction and resolved congestion

"In the design services market that AAI serves, fast turnaround time and predictability are critical requirements for the RTL-to-GDSII flow," said Bijan Kiani, vice president of marketing in Synopsys' Design Group. "The advanced RTL congestion analysis, synthesis-based design-for-test and low power implementation, coupled with physical guidance to IC Compiler II, enable our customers to achieve faster turnaround times for their critical SoCs while achieving superior quality of results and predictable silicon success."

About AAI

Avnet ASIC Israel Ltd. ("AAI") is a leading ASIC design center specializing in services for the design, layout and turn-key manufacturing of SoC ASIC devices, digital and mixed signal. AAI is a fully owned subsidiary of Avnet Inc. which is the world's number one distributor of electronic devices and technology services. AAI has been a cornerstone in the Israeli Semiconductor ASIC industry for over 25 years with over 350 successful designs serving both the Start-Up community as well as larger OEM's and in all segments of the local industry. AAI as vast experience with the leading Silicon Foundries in technology nodes down to 28nm and as well with various packaging solutions, design for test (DFT) techniques and production testing development. AAI is fully equipped with the leading tools from Synopsys and is fully geared to tackle the most challenging ASIC design projects from RTL to GDSII to Production Testing and Turn-Key Manufacturing.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software quality and security solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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