# Synopsys Launches Pre-Wafer Simulation Solution to Reduce Semiconductor Process Development Time

Enables Earlier Co-Optimization of Devices, Processes, Materials and Design

MOUNTAIN VIEW, Calif., May 23, 2016 /PRNewswire/ --

**Highlights:**

- Enables earlier narrowing down of process and device options, reducing expensive and time-consuming wafer-based iterations
- Allows creation of higher-quality early Process Design Kits (PDKs) for design technology co-optimization (DTCO)
- Targeted to advanced process nodes
- Early PDK enables IP designers to deliver more competitive products

Synopsys, Inc. (NASDAQ: SNPS) today announced a pre-wafer simulation solution to help semiconductor manufacturers reduce process node development time. The new solution provides a comprehensive process, transistor and circuit simulation flow that enables technology development and design teams to evaluate various transistor and process options using a design technology co-optimization methodology that starts in the pre-wafer research phase. The generation of SPICE models, design rules and parasitics from TCAD and lithography simulations allow the creation of early process design kits to evaluate the performance, power, area and cost of a new process node.

"To meet the performance, power, area and cost targets of the 10-nm process node and beyond, semiconductor manufacturers need to evaluate a larger number of process options, device architectures and materials, and account for design criteria in selecting the best options," said Dr. Anda Mocuta, Director of Technology Solutions and Enablement at imec. "The new simulation solution from Synopsys enables seamless links in the DTCO chain and helps speed up the down-selection of technology options," added Dr. Mocuta.

In the past, the development of new process nodes was focused on the scaling and optimization of a single device architecture, the planar MOSFET, and a single material, silicon. With the introduction of FinFET in logic and 3D-NAND in memory, the complexity of new process nodes increased significantly. This complexity will only accelerate as future process nodes will need to evaluate and select among a larger number of processes, device architectures and materials.

**Increasing Complexity of New Process Nodes**

- To meet the expected gains in performance, power and area with each new process node, current and next-generation lithography technologies must be evaluated from the point of view of critical pitches, pattern printability and layout constraints
- Achieving transistor performance and power targets requires consideration of new device architectures, such as nanowire FETs and tunnel FETs, with high-mobility channel materials as an option
- Selection among this exploding number of process, device architecture and material options is further complicated by complex interactions between design rules, interconnect parasitics, and transistor performance, and the unavailability during the early stages of research of wafer data from which to build or calibrate models

**Pre-Wafer Simulation Solution Benefits**

- Combines the production-proven Sentaurus TCAD, Process Explorer and Sentaurus Lithography tools with new tools for automated variation-aware SPICE model extraction
- Enables the creation of PDKs from simulation data so design teams can assess the impact of technology options on circuit performance and area earlier than currently possible
- By starting design-technology co-optimization earlier, process development teams can reduce expensive and time consuming wafer-based iterations when selecting the right options to meet process node performance, power, area, cost and timeline targets

"Working closely with our customers, we have developed a pre-wafer simulation solution to help our customers deliver process nodes faster," said Dr. Howard Ko, senior VP and general manager of the Silicon Engineering Group at Synopsys. "Our unique combination of TCAD, litho and SPICE simulation enables us to deliver a complete solution to address the challenges in technology development of advanced process nodes," added Dr. Ko.

**About Synopsys**

Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 16th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software quality and security solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

**Editorial Contact:**

Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

SOURCE Synopsys, Inc.