Synopsys' Custom Compiler Certified for TSMC 10-nm and 7-nm FinFET Process Nodes

TSMC and Synopsys collaborate to provide Custom Compiler-ready iPDKs

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Highlights:

- TSMC certifies Custom Compiler for 10nm and 7nm FinFET process technologies
- Custom Compiler supports new FinFET requirements such as track-pattern and full coloring flow
- Custom Compiler support for industry standard iPDKs enables custom design on a broad set of TSMC process technologies

Synopsys, Inc. (Nasdaq: SNPS) today announced that the company's new Custom Compiler™ tool (seetoday's news release) has been certified by TSMC for 10-nanometer (nm) FinFET production and for 7-nm early design starts. The certification ensures that Custom Compiler features supporting 10-nm and 7-nm FinFET technologies such as track-pattern support, coloring assistance, electrical-aware layout, EM/IR checking and parasitic-aware analysis are ready for mutual customers.

"A key part of our Custom Compiler development was to ensure tool readiness for the most advanced FinFET technology offered by TSMC," said Bijan Kiani, vice president of product marketing at Synopsys. "We created Custom Compiler to meet FinFET layout requirements and speed up FinFET layout tasks."

"We have worked closely with Synopsys to certify Custom Compiler for the 10-nanometer process node and 7-nanometer early design starts," said Suk Lee, TSMC senior director, Design Infrastructure Marketing Division. "A PDK is also available to support Custom Compiler for mutual customers on TSMC FinFET process nodes through the iPDK standard."

About Custom Compiler

Custom Compiler shortens the time it takes to complete FinFET design tasks from days to hours. Its visually-assisted automation leverages the graphical use model familiar to layout designers while eliminating the need to write complicated code and constraints. With Custom Compiler, routine and repetitive tasks are dealt with automatically without extra setup. Custom Compiler's visually-assisted automation provides four types of assistants: Layout, In-Design, Template and Co-Design. Layout Assistants speed layout with user-guided automation of placement and routing. In-Design Assistants reduce design iterations by catching physical and electrical errors before signoff verification. Template Assistants help designers reuse existing know-how by making it easy to apply previous layout decisions to new designs. Co-Design Assistants combine the IC Compiler™ place and route system and Custom Compiler into a unified solution for custom and digital implementation. Custom Compiler is based on the industry standard Open Access database. It provides an open environment spanning schematics, simulation analysis and layout. Unified with Synopsys' circuit simulation, physical verification and digital implementation tools, Custom Compiler provides a comprehensive custom design solution. For more information about Custom Compiler, visit https://www.synopsys.com/implementation-and-signoff/custom-implementation/custom-compiler.html .

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 16th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software quality and security solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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