# Synopsys' PrimeTime Speeds Timing and Power Closure for Complex SoC and IoT Designs

## Major Enhancements Enable Designers to Work Smarter for Faster Closure on FinFET Designs

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**Highlights:**

- 2X speedup, 16 core scalability and reduced need for costly path-based analysis (PBA) reporting significantly improves turnaround time (TAT)
- HyperScale technology proven to save schedule time and compute resources in more than 25 tapeouts
- Advanced Engineering Change Order (ECO) technology enables power reductions of up to 40 percent

Synopsys, Inc. (Nasdaq: SNPS) today announced that the 2015.12 release of the PrimeTime® static timing analysis tool provides major enhancements to address the challenges of timing and power closure for FinFET designs. New PrimeTime technology significantly improves turnaround time (TAT) and power reduction, while providing smarter utilization of compute resources. This software release helps ensure chip designers can meet demanding signoff schedules at advanced process nodes.

"In anticipation of designers' future timing closure challenges, Synopsys continues to offer smarter, more efficient technology," said Robert Hoogenstryd, senior director of marketing for design analysis and signoff tools at Synopsys. "The 2015.12 release of PrimeTime keeps our customers well ahead of the curve, providing significant reduction in turnaround time without requiring them to upgrade existing hardware."

System-on-chip (SoC) designers face pressure to close timing quickly, including reducing runtimes and finding necessary high-end compute resources. The latest release of PrimeTime takes a three-pronged approach to smarter and faster timing closure: First, it boosts performance, beginning with 2X overall faster run time and a 10X boost in reporting function speed. Second, PrimeTime provides improved scaling across 16 cores for 10-15X faster throughput compared to single core runs. Finally, tighter correlation of graph-based analysis (GBA) to path-based analysis (PBA), achieved through parametric on-chip variation (POCV) technology, means designers can spend less time doing runtime-costly PBA analysis to eliminate false violations.

"As a supplier of world-class computing solutions, our design teams must ensure our highly integrated semiconductor products achieve timing closure across a wide range of scenarios," said Bruce Fishbein, vice president of NCD IC engineering at Cavium. "Synopsys PrimeTime's continuously improving performance helps us meet our demanding signoff schedules."

With its HyperScale hierarchical methodology, the 2015.12 PrimeTime release reduces the need for expensive compute assets. HyperScale provides a 5-10X improvement in TAT and memory footprint compared to flat analysis, enabling use of more available and less costly compute servers. More than 20 tapeouts have successfully taken advantage of this technology.

"Mellanox's processing solutions excel at providing great flexibility and high performance, coupled with superior integration and power efficiency. Our engineers drive this innovation with on-time delivery of increasingly more advanced and complex designs," said Erez Shaizaf, vice president of chip design at Mellanox. "Our ability to meet signoff targets and get analysis runs through existing server farm resources requires an efficient combination of run time and memory. PrimeTime's HyperScale static timing analysis and ECO (engineering change order) technology delivers on both fronts."

For mobile and Internet of Things (IoT) applications, a few extra percent of power reduction can provide significant advantages in the consumer market. New PrimeTime ECO enhancements enable designers to squeeze out an additional 5 percent power reduction, for a total power reduction of up to 40 percent. Also included is support for complex placement rules, critical to 10-nanometer (nm) FinFET, that work in tandem with Synopsys' flagship IC Compiler™ II physical implementation tool. The PrimeTime ECO technology is deployed by more than 70 different companies over a broad set of applications.

At the SNUG® Silicon Valley conference, March 30-31, 2016, Synopsys will outline its vision of the next-generation of smarter signoff technology and numerous customers will share their success with PrimeTime.

**Availability and Resources**

PrimeTime 2015.12 is available now. For additional information, visit the Synopsys Galaxy™ Signoff Solution page, watch one of the many webinars or contact your local sales and support team.

**About Synopsys**

Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 16th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software quality and security solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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