TSMC Certifies Synopsys IC Compiler II for 10-nm FinFET Production and 7-nm Early Design Starts

Certification Includes Digital, Signoff and Custom Implementation Tools from Synopsys Galaxy Design Platform

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Highlights:

- IC Compiler II momentum is accelerated with TSMC certification at 10-nm
- Broad and deep collaboration made certification possible in significantly less time than previous technology nodes
- Advanced Waveform Propagation technology in the Galaxy Design Platform enables ultra-low voltage design in the new technology nodes

Synopsys, Inc. (Nasdaq: SNPS) today announced that TSMC has completed the certification for its most advanced 10-nanometer (nm) FinFET v1.0 technology node for a suite of Synopsys' digital, signoff and custom tools anchored by its IC Compiler™ II place and route solution. With multiple production designs already underway by early adopters of 10-nm, the certification paves the way for wide usage across the broad IC Compiler II installed base, enabling mutual customers to derive the maximum benefit from the new technology node. In addition, TSMC has already reached the first milestone of certification of IC Compiler II and related implementation tools for the latest design rule manual (DRM) and SPICE model of the 7-nm process node, allowing mutual customers to initiate early design activity.

To support TSMC 10-nm ultra-low voltage operation, Synopsys PrimeTime® is jointly enabled through the certification collaboration with TSMC for signoff analysis of waveform-sensitive ultra-low voltage operation. Additionally, the entire suite of tools from the Galaxy™ Design Platform is validated to handle the design rules and requirements of the full-colored 10-nm process, such as multiple patterning and reliability at all levels of the system-on-chip (SoC) design. The certified platform delivers routing rules, physical verification runsets, signoff-accurate extraction technology files, statistical timing analysis that correlates with SPICE, and interoperable process design kits (iPDKs) for the 10- and 7-nm FinFET processes.

"Our collaboration with TSMC on their 10- and 7-nm processes allows designers to confidently use the Galaxy Design Platform for their chip designs targeting TSMC's next-generation FinFET processes," said Bijan Kiani, vice president of product marketing of the Design Group at Synopsys. "The latest certification for both of these FinFET processes extends our deep relationship with TSMC for developing next-generation technologies."

"Building on our longstanding FinFET collaboration with Synopsys, this TSMC certification signifies that the tools from the Galaxy Design Platform are now ready for 10-nm production and early engagements for our mutual customers at 7-nm," said Suk Lee, TSMC senior director, Design Infrastructure Marketing Division. "The full-suite of TSMC-certified digital, signoff and custom implementation solutions from Synopsys will deliver high performance and lower power for our mutual customers."

Key Synopsys tools and features certified by TSMC include:

- IC Compiler II place and route: Advanced optimizations for the best area, timing and power quality of results (QoR) as well as support for power, signal and cell-level reliability analysis
- IC Validator signoff physical verification: Certified runsets for signoff DRC, LVS and metal fill; includes support for In-Design physical verification within Synopsys' IC Compiler II
- StarRC™ extraction: Multi-patterning, full color-aware variation and 3-D FinFET modeling for industry-leading signoff accuracy
- PrimeTime timing signoff: Ultra-low voltage timing signoff with Advanced Waveform Propagation (AWP), Liberty Variation Format (LVF)-based process variation analysis and placement rule-aware engineering change order (ECO) guidance
- Galaxy Custom Designer® schematic editor and Laker® layout editor: Support for full coloring flow; track-pattern support, in-design EM/IR calculation and integration with CustomSim™ EM/IR analysis for debugging layout signoff errors
- PrimeRail and CustomSim reliability analysis: Accurate static and dynamic gate-level and transistor-level analysis for color-aware electro-migration (EM) rules support for analysis and IR-drop integrity
- NanoTime custom timing analysis: SPICE-accurate transistor-level static timing analysis of 10-nm embedded SRAMs
- HSPICE®, CustomSim and FineSim® simulation: FinFET device modeling with self-heating effect and delivery of accurate circuit simulation results for analog, logic, high-frequency and SRAM designs
- ESP-CV custom functional verification: Transistor-level symbolic equivalence checking for 10-nm SRAM, macros and library cell designs

In addition, TSMC also collaborates with Synopsys on the DesignWare® STAR Memory System® product for test, repair and

diagnostics of FinFET-based memories.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 16th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software quality and security solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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