Synopsys Redefines Circuit Simulation with Native Environment

Eliminates Need for Third-party Environment, Accelerates Analog Verification

MOUNTAIN VIEW, Calif., Feb. 3, 2016 /PRNewswire/ --

Highlights:

- HSPICE, FineSim and CustomSim 2016.03 release to include native environment for analog verification
- Eliminates the need for third-party analog design environments
- Streamlines multi-testbench, multi-corner simulation setup, job monitoring and post simulation analysis
- Deployed at Samsung Electronics' System LSI Business for analog verification

Synopsys, Inc. (Nasdaq: SNPS) today announced that its circuit simulators will include a native environment for simulation management and analysis. Available in the 2016.03 release of HSPICE[®], FineSim[®] and CustomSim[™] simulators, the environment provides a comprehensive solution that improves analog verification productivity. The included solution provides designers with full access to the advanced features available in Synopsys SPICE and FastSPICE simulators and eliminates the need for third-party environments. As an early collaboration customer, Samsung Electronics' System LSI Business evaluated the new environment with FineSim SPICE and has deployed it to their analog design community.

Advanced-node designs must work across a wide range of voltages, operating conditions and have many modes of operation. To verify circuits under various operating conditions, design teams are running thousands of simulations and need to sort through massive amounts of data. To address this growing complexity, Synopsys has developed a comprehensive GUI-based transistor-level simulation and analysis environment that is deeply integrated with its circuit simulators and eliminates the need for any third-party environment.

Key capabilities of the environment include:

- · Netlist-based flow for direct import of SPICE, Verilog and DSPF
- Unified setup for corners, sweeps across multiple testbenches and Monte Carlo analysis
- Advanced job distribution and monitoring for batch mode simulations
- Integration with Synopsys' Custom WaveView™ graphical waveform viewer for extensive post-processing of waveforms
- Automated regression capability with industry-standard TCL scripting language
- Language-sensitive text editor for netlist-based navigation, cross-probing and syntax checking
- Advanced visual data navigation and data mining features such as charting, statistical analysis, histograms and scatterplots
- Detailed report generation, including web-based HTML documentation

"This upgrade to our circuit simulation portfolio provides a self-contained analog verification environment that improves circuit verification productivity and obviates the need for third-party tools," said Antun Domic, executive vice president and general manager at Synopsys. "Redefining what constitutes circuit simulation adds value to our customers' investment in our products and validates our commitment to deliver innovative solutions to address their circuit verification needs."

Synopsys will premiere a one-hour webinar "Improving Analog Verification Productivity Using Synopsys' Simulation and Analysis Environment (SAE)" on Wednesday, February 17, 2016 at 10:00 a.m. PST. This webinar provides an introduction to SAE and its key capabilities for improving productivity and throughput. The webinar will be available for on-demand viewing for the remainder of 2016.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 16th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software quality and security solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected release and benefits of the 2016.03 release of HSPICE, FineSim and CustomSim solutions. Any statements that are not statements of historical fact may be deemed to be forward-looking statements. These statements involve known and unknown risks, uncertainties and other factors that could cause actual results, timeframes or achievements to differ materially from those expressed or implied in the forward-looking statements. Other risks and uncertainties that may apply are set forth in the "Risk Factors" section of Synopsys' most recently filed Annual Report on Form 10-K. Synopsys undertakes no obligation to update publicly any forward-looking statements, or to update the reasons actual results could differ materially from those anticipated in these forward-looking statements, even if new information becomes available in the future.

Editorial Contact:

Monica Marmie Synopsys, Inc. 650-584-2890 monical@synopsys.com

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