Synopsys Launches New IP Subsystem to Accelerate Data Fusion Processing in IoT Devices

DesignWare Smart Data Fusion IP Subsystem Integrates Latest ARC EM DSP Processors, Peripherals and Software to Boost Signal Processing Performance and Reduce Energy Consumption

Disclaimer: GlobalFoundries acquired the Synopsys Processor Solutions business on June 1, 2026. Clickhere to learn more.

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Highlights:

- Integrated, pre-verified IP subsystem includes the latest power-efficient DesignWare ARC EM9D and EM11D processors for highly-efficient DSP performance
- Integrated microDMA controller provides 4X faster access times with lower system-level energy consumption by enabling data transfers during processor sleep modes
- Tightly-coupled memory, peripherals and hardware accelerators reduce power consumption by up to 85 percent compared to discrete solutions
- Software drivers and an extensive library of DSP functions such as FFT and DCT, FIR and IIR filters speed application software development
- New IP offering extends Synopsys' family of "Smart" subsystems optimized for IoT applications

Synopsys, Inc. (Nasdaq:SNPS) today announced the newDesignWare® Smart Data Fusion IP Subsystem, an integrated, pre-verified hardware and software IP product optimized for highly efficient DSP performance and ultra-low energy consumption. The Smart Data Fusion IP Subsystem offers a choice of DesignWare ARC® EM DSP processors, including the latest EM9D and EM11D cores with support for XY memory to boost signal processing performance. An integrated microDMA controller minimizes system-level energy consumption by enabling data transfers while the processor is in one of several programmable sleep modes. The integrated peripherals, memories, hardware accelerators and software DSP functions deliver the performance efficiency needed for common processing tasks in Internet-of-Things (IoT) applications such as always-on sensor fusion, voice and image detection and audio playback.

"IoT edge devices increasingly require a combination of low-power sensing capabilities and high-performance processing," said Tadaaki Yamauchi, vice president of the Core Technology Business Division at Renesas Electronics Corporation. "Through our collaborative demonstration platform, utilizing cutting-edge 40-nanometer embedded flash technology, Renesas and Synopsys show how designers can leverage complementary technologies such as Synopsys' DesignWare Smart Data Fusion IP Subsystem with Renesas' innovative, high-speed embedded flash memory controller IP to develop high-performance, cost-optimized IoT systems in less time."

The DesignWare Smart Data Fusion IP Subsystem is designed to process data from numerous digital and analog sensors with minimal power consumption, offloading the host processor and enabling more efficient processing of sensor data. The fully configurable IP subsystem includes an ARC EM5D, EM7D, EM9D or EM11D processor. This family of power-efficient cores combines RISC and DSP processing and includes support for XY memory banks to enable a sustained throughput of one 32x32 MAC operation (or two 16x16 MAC operations) per clock cycle. The additional signal processing bandwidth is optimized to manage the extensive data processing required by advanced sensor fusion algorithms and to improve processing efficiency for a range of audio formats including MP3, SBC, OPUS and AAC LC. For example, executing codecs such as Bluetooth Low Complexity Subband Coding (SBC) with ARC processors requires less than 40 microwatts of power in 40-nanometer low-power processes with frequency (MHz) requirements more than 25 percent lower than competitive processor offerings.

The subsystem's integrated microDMA controller enables memory and peripheral access during processor sleep modes and provides 4X faster access times compared to traditional bus-based DMA implementations. In addition, the subsystem incorporates highly-optimized I/O peripherals including multiple SPI, I^2C and analog-to-digital converter interfaces, further lowering gate count and energy consumption while reducing engineering effort.

To ease software development, the subsystem includes software drivers and a rich library of off-the-shelf DSP functions supporting filtering, correlation, matrix/vector, decimation/interpolation and complex math operations. Designers can implement these sensor-specific DSP functions in hardware using a combination of native DSP processor instructions and tightly coupled hardware accelerators to boost performance efficiency and reduce power consumption. The subsystem is supported by commercially available software covering a range of IoT functionality, including speech recognition, voice control, motion sensing and audio post-processing and playback. Additionally, Synopsys' embARC Open Software Platform gives software

developers online access to a comprehensive suite of free and open-source software that accelerates code development for the subsystem.

"Advanced sensor fusion applications require a high level of integration with minimal power consumption and area," saidJohn Koeter, vice president of marketing for IP and prototyping at Synopsys. "The new DesignWare Smart Data Fusion IP Subsystem gives designers a pre-verified hardware/software solution that delivers the additional DSP performance needed to manage specialized tasks like processing sensor information, recognizing voices and audio playback, while meeting the system's power budget. By delivering a complete, pre-integrated IP subsystem, we enable designers to quickly incorporate this key functionality into their IoT devices with significantly less risk and effort."

Availability

The DesignWare Smart Data Fusion IP Subsystem will be available inFebruary 2016.

Learn more about the Smart Data Fusion IP Subsystem:https://www.synopsys.com/dw/ipdir.php?ds=smart-data-fusion-subsystem

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit https://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 16th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software quality and security solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected release and benefits of the DesignWare Smart Data Fusion IP Subsystem. Any statements that are not statements of historical fact may be deemed to be forward-looking statements. These statements involve known and unknown risks, uncertainties and other factors that could cause actual results, time frames or achievements to differ materially from those expressed or implied in the forward-looking statements. Other risks and uncertainties that may apply are set forth in the "Risk Factors" section of Synopsys' most recently filed Annual Report on Form 10-K. Synopsys undertakes no obligation to update publicly any forward-looking statements, or to update the reasons actual results could differ materially from those anticipated in these forward-looking statements, even if new information becomes available in the future.

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