Synopsys' StarRC Raises the Bar in Parasitic Extraction Performance and Scalability

Smarter Resource Management Significantly Improves Customer Design Efficiency

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Highlights:

- 2X runtime speed up for faster extraction turnaround time (TAT)
- Simultaneous multi-corner (SMC) scalable to 200+ cores, with higher CPU efficiency
- 4X smaller disk usage through smarter resource management and seamless link to Synopsys' PrimeTime signoff solution

Synopsys, Inc. (Nasdaq: SNPS) today announced that the 2015.12 release of its StarRC™ solution delivers key technology innovations to address the increasing parasitic extraction and signoff challenges arising from Moore's Law scaling continuation. The new innovations significantly raise the bar on performance and scalability, while providing an improved architecture designed to leverage mainstream or leading-edge compute resources more efficiently. This latest release builds on StarRC's decade-plus industry leadership and continues the consistent delivery of productivity improvements to help IC designers meet their design, resource and schedule challenges.

"As our customers continue to push the design envelope, they are increasingly challenged to manage the rapidly growing design and multi-corner parasitic big data using their available resources," said Robert Hoogenstryd, senior director of marketing for design analysis and signoff at Synopsys. "The 2015.12 release of StarRC not only delivers greater performance, but also provides smarter and more efficient utilization of existing resources, while keeping an eye on the big picture, that is, enabling more productive timing analysis and signoff."

StarRC is the industry's premier parasitic extraction solution, trusted through thousands of tapeouts across broad application domains including mobile, data processing, communications, Internet of Things (IoT), automotive and more, and over multiple generations of process technologies including the latest 10-nanometer (nm) FinFET node. It offers a rich set of capabilities to enable the highest signoff performance, such as widely deployed SMC technology that allows designers to extract multiple corners in a single run and achieve up to 3X faster runtime using the same resources and with the same signoff accuracy.

The 2015.12 release of StarRC extends the performance benefits through additional architectural improvements to yield another 2X speedup and a significant boost in multi-core processing scalability, enabling the use of more CPU cores more efficiently. Design teams have already leveraged the improved runtime and scalability, combined with SMC technology, to extract hundreds of millions of instances on more than 200 CPU cores. Others have significantly accelerated the runtimes for their full-chip designs, completing eight corners of extraction for 350 million design instances in less than 3.5 hours or 100 million design instances per hour.

In addition, the 2015.12 StarRC release delivers the productivity benefits to the full signoff cycle with a unique new link to Synopsys' PrimeTime® signoff solution. The 2015.12 release of PrimeTime can directly read StarRC's golden multi-corner binary database, eliminating the need for parasitic netlist writing for multiple corners and saving up to 4X disk space, as well as enabling up to 20 percent speedup in signoff TAT. Design teams are already beginning to deploy this new solution and take advantage of disk savings, such as reducing disk size from more than 380 GB to under 90 GB for a large FinFET design. The reduction in disk space usage, combined with StarRC's proven memory efficiency of 8 GB per core, allows designers the flexibility to use more economical hardware in their environment to achieve significant cost savings and efficiency.

Availability

StarRC version 2015.12 is available now to licensed customers for download. For additional information, visit Synopsys' Galaxy Signoff Solution web page or contact your Synopsys Application Consultant representative.

About Synopsys

Synopsys, Inc. (Nasdaq: SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 16th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software quality and security solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications

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