Synopsys Platform Architect MCO Delivers Industry's First Power-Aware Architecture Analysis Tool Supporting IEEE 1801-2015 UPF 3.0

Solution Enables Efficient Reuse of UPF 3.0 System-Level IP Power Models for Early Analysis of SoC Architectures for Power and Performance

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Highlights:

- New IEEE 1801-2015 Unified Power Format (UPF) 3.0 standard enables the creation and reuse of interoperable system-level IP power models
- Platform Architect with support for IEEE 1801-2015 UPF 3.0 enables the addition of power analysis to existing architecture performance models without modification
- Unified view of activity, performance and power of multicore systems enables designers to understand how power management impacts system performance months earlier in the development cycle
- Platform Architect with multicore optimization technology accelerates power aware architecture design to reduce the risk of over-design and/or under-design

Synopsys, Inc. (Nasdaq:SNPS) today announced that its Platform Architect™ with Multicore Optimization (MCO) virtual prototyping solution is the first to support the new IEEE 1801-2015 Unified Power Format (UPF) 3.0 system-level IP power modeling standard. The new IEEE 1801-2015 UPF standard enables efficient creation and reuse of interoperable IP power models for early analysis of power and performance for multicore SoC architectures. Combined with Platform Architect MCO's native support for IEEE 1666-2011 SystemC transaction-level modeling (TLM) and Synopsys' Fast Timed (FT) model library, architects gain a unified view of system activity, performance and power to accelerate power-aware architecture design for multicore SoCs months earlier in the development cycle.

"As a user of Platform Architect MCO and a global supplier of high performance, low power memory technologies, Micron understands that early system-level analysis is critical to the successful design of energy-efficient SoCs and electronic products," said Bill Randolph, director of ecosystem enablement at Micron. "Synopsys' architecture design solution enables our customers to optimize and integrate SoC memory subsystems earlier in the development cycle, which helps speed the adoption of new technologies like our next-generation DDR4/LPDDR4 designs."

A system-level IP power model is an abstraction of the power behavior of a component that provides a specification of its power states and the associated power consumption data for each state. These abstracted power models enable early analysis of system-level power budgets and can be refined as more specific implementation information becomes available. To understand the impact of power management on system performance, architects and system designers must analyze power together with the simulation of realistic application workloads. Platform Architect MCO and its library of Fast Timed power aware architecture models provide this unified view based on fast simulation, quantitative analysis results and the ability to add power models without change. Together, this enables the efficient optimization of dynamic voltage frequency scaling (DVFS) power management policies and the partitioning of SoC power domains months before the complete RTL system is available.

"Architecture teams developing multicore SoCs must identify power and performance problems as early as possible to avoid under- and over-design," said John Koeter, vice president of marketing for IP and prototyping at Synopsys. "Synopsys' leading Platform Architect MCO tool provides immediate support for the new IEEE-1801 standards-based system-level IP power models and allows architects and system designers to define systems that yield the greatest energy efficiency."

Availability & Resources

Synopsys Platform Architect MCO supports the IEEE 1801-2015 UPF 3.0 system-level power modeling format now.

- Learn more about Platform Architect MCO: http://www.synopsys.com/platformarchitect

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 16th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also growing its leadership in software quality and security solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors,

or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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