Synopsys Enables Next-Level of Productivity with Addition of System-Level Capabilities to Verification IP for ARM Cache Coherent Protocols

Expands Comprehensive VIP library for ARM® AMBA® protocols with System-Level Test Suites, System Monitor, Protocol-aware Debug and Performance Analysis; Adds VIP for New AMBA 5 AHB5 Standard

MOUNTAIN VIEW, Calif., Nov. 10, 2015 /PRNewswire/ -- Synopsys, Inc. (NASDAQ: SNPS) announces the availability of advanced system-level capabilities in its next-generation VC Verification IP (VIP) for the ARM AMBA 4 ACE and AMBA 5 CHI protocols, as well as availability of verification IP for the newly announced AMBA 5 AHB5 protocol. The AMBA 4 ACE specifications are used for full coherency between processors, and AMBA 5 CHI is an architecture for system scalability in enterprise SoCs. The expanded capabilities of Synopsys Verification IP include system level test-suites, a system monitor, protocol-aware debug and performance analysis. With the growth of cache-coherent designs, checkers and performance analysis are required. The system-level capabilities of Synopsys VIP enable SoC teams to further accelerate time to first test and improve overall verification productivity.

"ARM and Synopsys have a long history of successful R&D collaboration on leading-edge verification products, including AMBA protocols," said Andy Nightingale, vice president of system IP marketing, systems and software group, ARM. "By adding system-level cache coherency VIP to support AMBA protocols, Synopsys is enabling our mutual customers to meet their aggressive targets and quickly bring innovative products to market."

Synopsys VIP features SystemVerilog source code test-suites, which include system-level coverage for accelerated verification closure. The VIP now also offers performance measurement metrics for in-depth analysis of throughput, latency and bottlenecks across cache coherent ports. Synopsys VIP also features system monitors, which interact with other VIP to ensure cache coherency across the system, accurate protocol behavior and data integrity.

Synopsys VIP is architected natively in SystemVerilog and UVM, is easy to use and can be integrated, configured and customized with minimal effort. It also supports native integration with Synopsys' Verdi® Protocol Analyzer, a graphical protocol-aware debug solution. As a result, Verdi Protocol Analyzer synchronizes high-level transactions to low-level signal activity across every layer of the AMBA protocol and custom cache coherent interconnects, providing system level debug support.

Synopsys also announced availability of verification IP for AMBA 5 AHB5 protocol. The new ARM AMBA 5 AHB5 protocol is an update to the widely adopted AMBA 3 AHB-Lite specification, enabling high-performance multi-master systems with support for exclusive transfers and additional memory attributes for seamless cache integration. The new AHB5 protocol also enables closer alignment with the AMBA 4 AXI protocol, enabling easier integration of AXI and AHB5 systems. AHB5 also adds support for secure/non-secure signaling.

"We have collaborated closely with ARM in creating Synopsys VIP for system-level verification of AMBA protocols, helping leading-edge SoC design teams address the increasing complexity of coherency verification," said Debashis Chowdhury, vice president of R&D at Synopsys Verification Group. "Our next-generation VIP helps designers accelerate verification closure and time to market as well as increase design quality."

For more information about Synopsys VIP and its support of AMBA protocols:

- Visit our booth at ARM TechCon on November 11-122015
- Listen to our webinar on VIP support for ARM Cache Coherent Interconnects on November 18, 2015

About Synopsys Verification IP

Synopsys VC VIP, based on its next-generation architecture and implemented in native SystemVerilog and UVM, offers native performance, native debug with Verdi Protocol Analyzer, ease of use, complete configurability and comprehensive coverage. These capabilities substantially increase user productivity for one of the most difficult and time-consuming aspects of SoC design and verification. The Synopsys VC VIP library includes a broad portfolio of interface, bus and memory protocols. More information is available at www.synopsys.com/vip.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 16th largest software company, Synopsys has a long

history of being a global leader in electronic design automation (EDA) and semiconductor IP and is also a leader in software quality and security testing with its Coverity® solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Editorial Contacts:

Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

SOURCE Synopsys, Inc.