New Release of Synopsys Synplify Software Delivers Up to 3X Faster Runtime with Higher FPGA Performance

Latest Enhancements Provide up to 10 Percent Increase in Quality of Results and Accelerate Development of High Reliability and Functional Safety Designs

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Highlights:

- New parallel synthesis execution capability delivers up to 3X faster runtime with smaller area and higher performance
- Physically-aware advanced synthesis provides up to 10 percent improvement in timing quality of results enabling smaller, faster and more cost-effective FPGA designs
- Enhanced triple modular redundancy, safe finite state machine and error handling features automate and accelerate development of high reliability designs
- Automated IP import capabilities and support for reading IEEE P1735 encrypted IP accelerates incorporation of internally developed and third-party IP

Synopsys, Inc. (Nasdaq:SNPS) today announced the availability of the latest release of the Synopsys Synplify Pro® and Synplify® Premier FPGA synthesis software tools. This release includes new multiprocessing technology that accelerates runtime by up to 3X compared to the previous generation and physically-aware advanced synthesis to increase timing quality of results (QoR) by up to 10 percent. This new technology enables automatic integration of IP from multiple sources allowing designers to utilize the optimal FPGA device for their product. The latest release also delivers enhancements to accelerate development of fault-tolerant systems, utilizing enhanced support for triple module redundancy (TMR), safe and fault-tolerant finite state machine (FSM) and error monitoring and handling. These improvements help accelerate the design of FPGAs for high reliability and safety critical applications operating in harsh and high radiation environments in the medical, automotive, industrial, space and communications markets.

Synplify's new multiprocessing technology enables the use of a single software license to automatically compile designs utilizing multiple cores on an individual machine or distributed to many machines. In addition, support for physically-aware advanced synthesis, which utilizes placement-aware optimizations within the designer's existing logic synthesis flow, improves timing QoR by up to 10 percent compared to the previous logic synthesis method in the Synplify tool. Synplify's runtime advancements enable faster implementation of complex FPGAs and deliver instant productivity to prototyping teams building their own FPGA-based prototyping flow.

"Our customers are developing increasingly complex systems and require tools that help them complete their designs faster," said Alex Grbic, senior director of marketing for software, DSP and IP at Altera. "The latest runtime and physically-aware advanced synthesis capabilities in Synopsys' Synplify software tools, combined with the fast runtimes of Altera's Quartus II software provide our mutual customers with a faster path to completing designs using Arria 10 FPGAs and SoCs."

The increasing complexity of FPGA devices creates a challenge for designers integrating IP from multiple sources. Synplify has been enhanced with automated IP import capabilities and support for reading IEEE P1735 encrypted IP, enabling designers to quickly incorporate a broad range of internally developed, third party and FPGA vendor IP into their systems with less effort and lower risk.

"We have been working closely with Synopsys for many years to ensure the seamless integration between Synplify and the Vivado Design Suite for customers using our FPGAs," said Tom Feist, senior marketing director of design methodology at Xilinx. "In particular, the new IEEE P1735 encryption support offered in the latest Synplify release has greatly helped our customers accelerate the integration of Xilinx IP into our UltraScale FPGAs."

Synplify Premier software automatically builds in fault tolerance and error mitigation to help FPGA designers create products that mandate highly reliable operation. Synplify Premier automates the process of creating circuitry using a combination of advanced features, which greatly accelerates productivity beyond manual implementation. These features include selective triple modular redundancy (TMR), fault-tolerant error correcting code (ECC) memory inference and the creation of finite state machine (FSM) utilizing Hamming-3 encoding for detection and correction of radiation-induced soft errors.

"As FPGAs increase in complexity, the need for synthesis tools that provide fast design turnaround time, increased performance and highly reliable operation are essential for FPGA designers," said John Koeter, vice

president of marketing for IP and prototyping at Synopsys. "The new features in Synplify significantly accelerate FPGA-based product designs, enabling the design of large-scale FPGAs with the smallest area and highest performance, while also providing immediate benefit to prototyping teams building their own FPGA-based prototyping flow."

Availability and Resources

The latest release of the Synplify Pro and Synplify Premier synthesis software is available now. Customers with a current maintenance agreement can download this new version from Synopsys using their SolvNet® account.

Learn more about Synplify Implementation tools:

- http://www.synopsys.com/fpga

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 16th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP, and is also growing its leadership in software quality and security solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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