Synopsys Unveils New ATPG Technology Delivering 10X Faster Test Pattern Generation

Innovative, Efficient Engines Achieve Speed-Up While Reducing Pattern Count by 25 Percent

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Highlights:

- Memory-efficient, multithreaded engines utilize available server cores to speed up automatic test pattern generation (ATPG) and silicon diagnosis
- Twenty-five percent fewer test patterns reduce test time and cost
- Tight links with the Galaxy Design Platform tools to deliver the highest quality test

Synopsys, Inc. (Nasdaq: SNPS) today announced a new, breakthrough ATPG and diagnostics technology that delivers 10X faster run time and 25 percent fewer test patterns to shorten schedules, accelerate silicon debug and reduce test time and cost. Innovative, memory-efficient engines for test generation, fault simulation and diagnosis execute finely segmented threads on all available server cores, maximizing throughput while minimizing the number of patterns required to achieve targeted test coverage. Combined with Synopsys' DFTMAX™ compression, this new test technology will enable design teams to meet their test quality, time and cost goals with unprecedented speed.

"Increasingly complex SoC designs and shrinking schedules require fast turn-around for generating high-quality manufacturing test patterns," said Roberto Mattiuzzo, SoC integration and DFT methodologies manager in STMicroelectronics' Digital and Mixed Processes ASIC division. "Working with Synopsys on their new ATPG technology should produce faster ATPG run times and significantly fewer test patterns to help us test first-silicon samples sooner and minimize time on the tester. This technology will also help accelerate our ramp-up of dense and complex products in FD-SOI technology thanks to an even more efficient flow for our ASIC customers."

The new test generation, fault simulation and diagnosis engines are extremely fast, exceedingly memory efficient and highly optimized for generating patterns and executing fine-grained multithreading of the ATPG and diagnosis processes. These innovations lead to fewer test patterns and 10X faster runtime, enable utilization of all server cores regardless of design size and surpass previous technologies that are limited by high memory usage. Moreover, tight links with Synopsys' Galaxy™ Design Platform tools, such as Design Compiler® RTL Synthesis, PrimeTime® timing signoff and StarRC™ parasitic extraction, along with other Synopsys tools, including Yield Explorer® yield analysis and Verdi® automated debug system, deliver the highest quality test while minimizing turnaround time.

"Customers worldwide rely on Synopsys' synthesis-based test solution to achieve the highest test quality on their most challenging designs," said Antun Domic, executive vice president and general manager for Synopsys' Design Group. "This announcement demonstrates our commitment to continually deliver innovative and groundbreaking test technologies, and addresses our customers' need for faster ATPG and diagnostics as well as reduced silicon test time."

About the Synopsys Synthesis-Based Test Solution

The Synopsys synthesis-based test solution is comprised of SpyGlass® DFT ADV testability analysis, DFTMAX, DFTMAX Ultra and TetraMAX® power-aware logic test and silicon diagnostics offerings; the DesignWare® STAR Hierarchical System for hierarchical test of IP and cores on an SoC; the DesignWare STAR Memory System® solution for embedded test, repair and diagnostics; the Yield Explorer® tool for design-centric yield analysis; and the Camelot™ software system for CAD navigation. Synopsys' test solution combines Design Compiler RTL synthesis with embedded test technology to optimize timing, power, area and congestion for test as well as functional logic, leading to faster time-to-results. The Synopsys test solution delivers tight integration across the Synopsys Galaxy Design Platform, including Design Compiler, IC Compiler™ II place and route system, and PrimeTime, to enable faster turnaround time meeting both design and test goals, higher defect coverage and faster yield ramp.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 16th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP, and is also a leader in software quality and security testing with its Coverity® solutions.

Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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