Fuji Xerox Reduces Silicon Area by More than 50 Percent Using Synopsys ASIP Designer

Synopsys' Application-Specific Instruction-Set Processor Tool Enabled Rapid Exploration and Optimization of Processor Architecture for Multi-Function Printer Application

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Highlights:

- Fuji Xerox reduced silicon area by more than 50 percent using an application-specific instruction set processor (ASIP) developed with ASIP Designer, compared to fixed hardware
- ASIP Designer's "compiler-in-the-loop" technology enabled use of application code to optimize the processor architecture for performance, power and area
- Automatic generation of software development kit and synthesizable RTL enabled Fuji Xerox to complete the entire design in less than 14 months

Synopsys, Inc. (Nasdaq:SNPS) today announced Fuji Xerox Co., Ltd. used Synopsys' ASIP Designer tool to design a high-performance application-specific instruction set processor (ASIP) for its full-color multifunction printer. With ASIP Designer, Fuji Xerox developed a specialized instruction-set custom processor that consumed less than 50 percent of the die area of a fixed hardware implementation while still meeting the performance requirements. In addition, unlike fixed hardware, an ASIP offers software programmability, providing the flexibility Fuji Xerox needed to meet the varied processing demands of its multifunction printer application. Using ASIP Designer, Fuji Xerox's design team was able to complete its ASIP design from concept to implementation in less than14 months.

"Synopsys' reputation as the premier provider of ASIP development tools was the key factor in our decision to use ASIP Designer for our custom processor development," said Noriaki Tsuchiya, manager of the Controller Development Group at Fuji Xerox Co., Ltd. "ASIP Designer's rapid architectural exploration capability made it possible for us to immediately profile the architecture against our algorithms. Designing an ASIP with an instruction set and functional units tailored to our application domain enabled us to significantly reduce gate count, while achieving our required system performance of printing 70 pages per minute."

While angularity correction is typically done mechanically, the need for quiet operation in office automation equipment required Fuji Xerox to take the different approach of using advanced image processing algorithms to apply the correction to the scanned image. To implement this in a performance- and area-efficient way, with the flexibility to make modifications to the algorithm, Fuji Xerox chose to design a custom processor using Synopsys' ASIP Designer tool.

Synopsys' ASIP Designer allowed Fuji Xerox to use a high-level specification of the processor to quickly model multiple processor architectures. Using this single input specification, ASIP Designer automatically configured the software development kit (SDK) containing an instruction-set simulator (ISS), assembler, linker, debugger and C compiler, and also generated the synthesizable RTL design. The immediate availability of the C compiler and the ISS, including its advanced profiling capabilities, enabled the unique "compiler-in-the-loop" methodology, allowing Fuji Xerox to rapidly profile the performance and tune the architecture for its specific image processing algorithms written in C.

"By replacing fixed hardware with ASIPs, companies like Fuji Xerox can significantly reduce total system cost, while increasing the overall flexibility of the design," said John Koeter, vice president of marketing for

IP and prototyping at Synopsys. "Fuji Xerox's implementation of an ASIP for image correction in their multi-function printer illustrates how Synopsys' ASIP Designer tool enables designers to rapidly explore and optimize processor architectures to achieve the best balance of programmability, performance and area, while accelerating the development of their SoC."

Resources

- Read the success story: http://www.synopsys.com/IP/Pages/fuji-xerox-success-story.aspx
- Learn more about Synopsys' ASIP design tools at http://www.synopsys.com/ASIP

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 16th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP, and is also growing its leadership in software quality and security solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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