# TSMC Certifies Synopsys' IC Compiler II on 10-nanometer FinFET Process

Collaboration Delivers Tool Enablement for Mutual Customers

MOUNTAIN VIEW, Calif., Sept. 16, 2015 /PRNewswire/ -- Synopsys, Inc. (Nasdaq:SNPS) today announced that TSMC has certified its IC Compiler™ II place and route product for V0.9 of 10-nanometer (nm) FinFET process technology (N10FF), and are on track to work towards V1.0 completion in Q4, 2015. IC Compiler II is the successor to IC Compiler, the place and route solution for advanced designs, delivering an improvement in throughput while achieving quality-of-results (QoR) that meets TSMC's certification requirements.

IC Compiler II is a place and route system built from the ground up to deliver improvement in design turnaround. Its new, highly innovative technology infrastructure includes data model, library and core engine advances that maximize multi-core and multi-machine scalability. Patented adaptive abstraction and compact data encapsulation technologies deliver capacity for large scale design planning tasks while concurrently achieving faster implementation.

With QoR being a key focus during its development, IC Compiler II features an analytical physical synthesis engine, variation-tolerant clock-building techniques, and solver-driven post-route optimization, which together deliver standard-setting timing, area and power benefits. Balancing innovation with strategic reuse of technologies in IC Compiler, IC Compiler II deploys the Zroute router and linear-gradient placer. These components enable day-one availability of technology files, along with a solid foundation to meet the stringent TSMC 10-nm requirements, including: full coloring flow enablement; vertically-constrained placement; layer-based optimization; low-Vdd timing-closure; and signal electromigration.

"TSMC continues to push the limits of physics to enable faster, smaller and more energy-efficient silicon solutions, it is imperative that we work closely with them to accelerate design enablement," said Bijan Kiani, vice president of marketing for the Design Group at Synopsys, Inc. "Through our partnership with TSMC on its 10-nanometer process, we are ensuring that our mutual customers are successful at bringing innovative and exciting products to market at the new node faster than ever before."

"10 nanometer is TSMC's next-generation FinFET process that delivers significant power, performance and area benefits across a broad range of design types and styles for the most demanding SoC applications," said Suk Lee, TSMC Senior Director, Design Infrastructure Marketing Division. "Through close collaboration with Synopsys, and our rigorous testing and certification of IC Compiler II, we are able to provide designers with a high-quality design enablement solution."

**About Synopsys**

Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 16th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP, and is also a leader in software quality and security testing with its Coverity® solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

**Editorial Contacts:**
Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.
650-968-8900 ext. 115
lgmartin@mcapr.com

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