New DesignWare ARC EM Processors Deliver Up to 3X Higher DSP Performance

ARC EM9D and EM11D Cores Address Need for Increasing Signal Processing Bandwidth in IoT Applications

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Highlights:

- Latest cores extend the ARC EM DSP Processor Family, combining high efficiency control and signal processing for ultra-low power, always-on applications
- New XY memory support in EM9D and EM11D delivers up to 3X or more DSP performance than existing ARC EM processor cores, with lower energy consumption
- Enhanced ARC MetaWare Development Toolkit and DSP library provide flexible C/C++ programming to ease application software development

Synopsys, Inc. (Nasdaq: SNPS) today announced availability of the DesignWare® ARC® EM9D and EM11D Processors, the newest additions to the power-efficient ARC EM Family of processors. The EM9D and EM11D cores implement an enhanced version of the ARCv2DSP instruction set architecture (ISA), combining RISC and DSP processing with support for an XY memory system to boost digital signal processing performance while minimizing power consumption. The cores maximize processing throughput by retrieving instructions and data from memories that are tightly coupled to the processor pipeline, reducing the number of accesses to system memory along with the associated latency and power consumption penalties. The ARC MetaWare Development Toolkit has been enhanced to offer full C/C++ programming support for the cores' DSP instructions and XY memory as well as a rich library of DSP functions to facilitate software development. The new cores are optimized for DSP-intensive functions such as sensor fusion, voice detection, speech recognition and audio processing that are common in Internet of Things (IoT) and other embedded applications.

"Synopsys' ARC EM9D and EM11D processors are ideally suited for the increasing number of IoT devices using speech comprehension capabilities to enhance hands-free operation," said Dean Neumann, CEO at Malaspina Labs. "The combination of these latest ARC EM cores and highly efficient speech processing software such as Malaspina Labs' VoiceBoost suite delivers an ultra-low power solution for voice activation, biometric verification and speech recognition in 'always listening' devices."

The ARC EM9D and EM11D cores deliver the highest level of digital signal processing performance to date in the ARC EM DSP Processor family. All EM DSP cores implement a three-stage pipeline and are ideal for applications with a mixture of control and DSP workloads. The EM9D and EM11D take advantage of regular data access patterns common in signal processing code by integrating separate X and Y memories with hardware support for address generation and DMA to move data in and out of the memories. This enables a sustained throughput of one 32x32 MAC operation or two 16x16 MAC operations per clock cycle with minimal energy and area overhead. These new processors have also been enhanced to support full integer, fractional divide and square root operations, unaligned loads/stores and bitstream parsing. These features enable the EM9D and EM11D to deliver the additional DSP performance required to execute complex sensor algorithms, as well as improve processing efficiency for a range of audio formats including MP3, SBC, OPUS and AAC LC. For example, the logic power consumption of the EM9D performing MP3 decode at 44.1 kHz, 128 kbps on a 28-nanometer process (nominal) is less than 40 microwatts.

The new EM9D and EM11D, like all ARC processor cores, are supported by the DesignWare ARC MetaWare Development Toolkit, a complete suite of tools for developing, debugging and optimizing software targeted for ARC processors. New features to ease DSP programmability and optimize applications for use with the XY memories have been added to the latest MetaWare release. For regular C code, the compiler automatically generates ARCv2DSP ISA instructions to deliver better performance, including guided and auto vectorization optimizations. Programmers can also efficiently target the cores' DSP and XY memory resources directly through the use of C code with qualifiers and primitives and by making use of the MetaWare Compiler's ability to automatically generate references to XY memory. The MetaWare Toolkit includes a rich library of DSP functions such as FFT and DCT, FIR and IIR filters, as well as vector and matrix math functions, allowing software engineers to rapidly implement algorithms from standard DSP building blocks. The toolkit also includes an ITU-T base-ops library for developing voice codecs. For further DSP optimizations, programmers can take advantage of available native fixed-point data types, C++ wrapper classes and an API for fixed-point math primitives. Intrinsics can be used to manually optimize code for maximum performance and power savings.

In addition, the embARC Open Software Platform gives all ARC EM software developers online access to a comprehensive suite of free and open-source software that eases the development of code for IoT and other embedded applications.

"Today's connected devices draw information from multiple sensors and must respond almost instantly, requiring an increasing amount of processing bandwidth without draining their batteries," said John Koeter, vice president of marketing for IP and prototyping at Synopsys. "The increased DSP bandwidth of Synopsys' ARC EM9D and EM11D processors gives designers of always-on devices the dual benefits of higher performance for more DSP-intensive tasks and the ability to conserve power by running at lower clock frequencies."

Availability and Resources

The ARC EM9D and EM11D processors and associated MetaWare software development tools are scheduled for general availability in September, 2015.

- Learn more about the ARC EM DSP processors: https://www.synopsys.com/dw/ipdir.php?ds=arc-em9d-em11d

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, wired and wireless interface IP, security IP, embedded processors and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 16th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP, and is also growing its leadership in software quality and security solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Forward-Looking Statements

This press release contains forward-looking statements within the meaning of Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected release and benefits of the DesignWare ARC EM9D and EM11D processors. Any statements that are not statements of historical fact may be deemed to be forward-looking statements. These statements involve known and unknown risks, uncertainties and other factors that could cause actual results, time frames or achievements to differ materially from those expressed or implied in the forward-looking statements. Other risks and uncertainties that may apply are set forth in the "Risk Factors" section of Synopsys' most recently filed Quarterly Report on Form 10-Q. Synopsys undertakes no obligation to update publicly any forward-looking statements, or to update the reasons actual results could differ materially from those anticipated in these forward-looking statements, even if new information becomes available in the future.

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