Synopsys' Design Compiler Graphical Adopted by Renesas for Automotive ICs

Achieves Higher Frequency and Smaller Area

MOUNTAIN VIEW, Calif., Sept. 9, 2015 /PRNewswire/ -- **Highlights:**

- Design Compiler Graphical deployed for implementation of Renesas designs.
- Significant reduction in routing congestion leads to faster timing and smaller area.
- Congestion optimization and tight correlation to IC Compiler deliver faster design closure.

Synopsys, Inc. (Nasdaq: SNPS), today announced that Renesas, a leading solution provider delivering highly reliable and high-safety products for automotive, has deployed Synopsys' Design Compiler® Graphical solution for their designs. Improving performance, while reducing power and area, is critical for Renesas to offer high performance balanced with very low power consumption over a wide and scalable range of products. To achieve these goals, Renesas deployed a design flow that combines Design Compiler Graphical and Synopsys' IC Compiler™ place-and-route solution.

"As exciting infotainment and safety options become significant criteria in the purchase of new products, our customers are looking to Renesas to deliver higher performance, energy-efficient products to market," said Tatsuji Kagatani, manager of Design Automation Department at Renesas System Design Co., Ltd. "Design Compiler Graphical's significant area and routing congestion reduction, combined with IC Compiler for place and route, enable our design teams to achieve faster timing and smaller area. We have widely deployed Design Compiler Graphical for our products currently using our 40-nanometer process."

Design Compiler Graphical addresses challenging requirements, such as performance, area, power and congestion, at all process nodes. It provides IC designers with visualization of congested circuit regions and performs automated synthesis optimizations to minimize congestion in these areas. Additionally, new optimization technologies monotonically reduce design area and leakage power by an average of 20 percent while maintaining timing QoR. Design Compiler Graphical shares physical technologies with IC Compiler and IC Compiler II place-and-route solutions to deliver highly correlated results for timing, area, power and routability, reducing design iterations and shaving critical schedule time.

"In the automotive market that Renesas serves, performance, low power consumption and cost-effectiveness are essential goals for their designers," said Bijan Kiani, vice president of marketing in Synopsys' Design Group. "Design Compiler Graphical's advanced optimization technologies and tight links with IC Compiler enable Renesas to deliver differentiated, high-performance products to market quickly."

About Synopsys
Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 16th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP, and is also growing its leadership in software quality and security solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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