Synopsys' IC Validator Signoff Physical Verification Delivers 2X Memory Reduction in Latest Release

Reduced Memory, Improved Runtime and Broad Runset Availability Driving Adoption by Leading Companies

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Highlights:

- Delivers 2X memory reduction
- Achieves 20 percent faster DRC checking on large designs
- Includes new four-color patterning decomposition and verification engine
- Offers certified signoff runsets for all major foundries
- Enables timing-aware track-based metal fill with IC Compiler II

Synopsys, Inc. (Nasdaq:SNPS) today announced the 2015.06 release of its comprehensive physical verification signoff product, IC Validator. The 2015.06 release focuses on refinements to the core engines to deliver a 2X memory footprint reduction. With IC Validator 2015.06, designers can extend the use of their current workstations and manage multiple concurrent jobs with greater ease. The new release delivers 20 percent faster signoff DRC performance on average and is as much as 2X faster in many cases. IC Validator extends support for emerging process nodes and FinFET technology with new four-color patterning decomposition and verification support. Certified signoff runsets at 28 nanometers (nm) and below for all major foundries are available today.

IC Validator is the key technology enabler for In-Design physical verification in the IC Compiler™ and IC Compiler II place and route solutions. IC Validator In-Design in the 2015.06 release introduces timing- and density-aware track-based metal fill that offers higher density than foundry fill while maintaining pre-fill design timing. Additionally, In-Design automated DRC repair (ADR) refinements now deliver a fix rate of greater than 80 percent, with many designs achieving fix rates of 100 percent.

Advances in process technology and ever-increasing design complexity have placed growing demand on physical verification products to check many more design rules. This evolution has created intense interest among IC designers in a new physical verification solution geared specifically to address these challenges. IC Validator is a comprehensive physical verification product including design rule checks (DRC), layout-vs.-schematic (LVS) checks, programmable extended electrical rule checking (EERC) and metal fill insertion. IC Validator's modern architecture and excellent multi-core scalability make it the signoff tool of choice for a growing number of designers, from those developing small analog chips to those designing the largest, most advanced digital chips.

"We are committed to providing the best physical verification signoff solutions for our customers working with the leading foundries and at the latest emerging technology nodes," said Bijan Kiani, vice president of marketing for Synopsys' Design Group. "A growing number of leading customers are adopting IC Validator and realizing the advantages of In-Design when tackling their growing physical verification challenges."

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 16th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP, and is also a leader in software quality and security testing with its Coverity® solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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