Key ASIC Deploys Synopsys' Design Compiler Graphical to Accelerate System-on-Chip Design

Delivers Higher Frequency and Smaller Area Compared to Other Synthesis Solutions

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Highlights:

- Key ASIC has deployed Design Compiler Graphical to accelerate the design implementation of its consumer, wireless and personal electronics ICs
- Comprehensive evaluation of available synthesis tools demonstrated Design Compiler Graphical's benefits of improved timing QoR (Quality of Results) and area reduction
- Tight correlation between Synopsys' Design Compiler Graphical and IC Compiler enable Key ASIC to identify timing issues early and accelerate design schedule

Synopsys, Inc. (Nasdaq: SNPS), today announced that Key ASIC, a leading supplier of wireless storage solutions and a design and manufacturing service provider specializing in customer-specific system products (CSSPs) and high-performance, low-power ASICs, has deployed the Synopsys Design Compiler® Graphical RTL synthesis solution to accelerate system-on-chip (SoC) design. Achieving high performance, low power and small die size results are primary objectives for Key ASIC to enable quick and cost-effective tapeouts. After a comprehensive evaluation of available synthesis solutions, Key ASIC found the most appropriate tool combination for their design needs is Design Compiler Graphical and Synopsys' IC Compiler™ place-and-route solution, which consistently deliver better timing QoR and smaller area.

"Key ASIC's design expertise targets the critical challenges of smaller die size, functional integration and cost reduction for high-performance, low-power SoCs," said Meisie Jong, general manager of Key ASIC's Technology Services business unit. "With Design Compiler Graphical we can identify and fix timing issues in a timely manner during synthesis and achieve higher frequency and smaller area faster. Based on our evaluation experience, we have now deployed Design Compiler Graphical as part of our production design flow."

Design Compiler Graphical addresses challenging requirements, such as performance, area, power and congestion, at both established and emerging process nodes. It provides IC designers with visualization of congested circuit regions and performs automated synthesis optimizations to minimize congestion in these areas. Additionally, new optimization technologies monotonically reduce design area and leakage power by an average of 20 percent while maintaining timing QoR. Design Compiler Graphical shares physical technologies with Synopsys' IC Compiler and IC Compiler II place-and-route solutions to deliver highly correlated results for timing, area, power and routability, reducing design iterations and shaving critical schedule time.

"Key ASIC's solutions and the customers they serve require the best combination of performance, low power and small die size to be competitive and cost-effective in the market," said Bijan Kiani, vice president of marketing in Synopsys' Design Group. "Design Compiler Graphical's market-leading synthesis technologies and tight correlation with IC Compiler enable Key ASIC to focus on their design expertise and unique IP while achieving the best quality of results and reduced tapeout schedules."

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP, and is also a leader in software quality and security testing with its Coverity® solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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