

Synopsys PCI Express IP Adds System-Level Data Protection Features for High-Performance Cloud Computing SoCs

Supports Latest 16G PCIe 4.0 Specification and Adds Features for Reliability, Availability and Serviceability

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Highlights:

- DesignWare IP for PCI Express delivers critical reliability, availability and serviceability (RAS) features to increase data protection, system availability and issue diagnosis for high-performance, data-intensive cloud applications
- Support for the new PCIe 4.0 v0.5 specification gives designers the ability to start incorporating the latest functionality while meeting high-performance 16 GT/s data transfer speeds
- Synopsys will demonstrate its complete PCIe 4.0 IP solutions, including controller, PHY and verification IP, at the PCI-SIG Developers Conference 2015 in Santa Clara, CA, June 23-24, 2015

Synopsys, Inc. (Nasdaq:SNPS) today announced that it has extended its DesignWare® IP solution for [PCI Express® \(PCIe®\) 4.0](#) to support RAS features to help designers ensure data integrity and increase data protection in cloud computing SoCs. The new RAS features increase system reliability by using parity and error correcting code (ECC) data protection in conjunction with protocol-defined mechanisms to detect and correct errors in the datapath and RAMs. Event counters and statistics monitor system availability, while error injection and silicon debug capabilities help diagnose issues and validate system recovery.

Designers of enterprise systems require increasing levels of bandwidth and that is driving designers to adopt the latest versions of the 16 GT/s PCIe 4.0 specification. Even while the PCIe 4.0 specification is under development, Synopsys performs extensive interoperability testing with ecosystem partners to help designers reduce design risk for their initial products with PCIe 4.0.

"Our successful PCIe 4.0 system interoperability with Synopsys demonstrates the robustness of both the specification and our products," said Alon Webman, vice president of silicon engineering, at Mellanox Technologies. "The PCIe 4.0 specification, supported by industry leaders like Synopsys and Mellanox as well as the full PCI Express ecosystem, will support the requirements of enterprise applications to handle ever-increasing amounts of data."

"Teledyne-LeCroy works closely with Synopsys to ensure interoperability between our respective market-leading solutions and to ensure compliance to the latest PCIe specifications," said John Wiedemeier, product marketing manager at Teledyne-LeCroy. "By starting interoperability testing early in the specification development process and continuing through specification updates, Teledyne-LeCroy and Synopsys are giving designers confidence that the IP will work as expected, thereby reducing their design risk."

The DesignWare Controller IP for PCIe 4.0 supports multiple lanes (x1 to x16) and multiple datapath widths for optimal configurations, as well as Native, ARM® AMBA® AXI-3™ and AMBA AXI-4™ interfaces for easy integration into systems-on-chips (SoCs). The DesignWare PHY IP for PCIe 4.0 supports full-featured bifurcation and aggregation, offering designers the flexibility either to configure the PHY macro into multiple individual links at 2.5, 5, 8 or 16 GT/s, or to aggregate the PHY macro up to 16 lanes. Synopsys PCI Express 4.0 Verification IP is based on a 100 percent SystemVerilog, UVM-based architecture with test suites delivered as source code to enable quick development of a verification environment to verify the proper integration and connection of the PCIe interface within the SoC.

"RAS is growing in importance in high-performance cloud computing applications to ensure the data integrity of terabytes of data," said John Koeter, vice president of marketing for IP and prototyping at Synopsys. "As the leading provider of PCI Express IP, Synopsys continues to invest in PCIe IP to enable designers to integrate the latest versions of the PCIe specification and provide the RAS features needed for data-intensive SoCs."

Availability & Additional Information

The DesignWare Controller and Verification IP for PCI Express 4.0 are available now. For availability information on the DesignWare PHY IP for PCI Express 4.0, please contact Synopsys. DesignWare IP Prototyping Kits for PCI Express are also available now.

Synopsys will demonstrate its PCIe 4.0 IP solutions and interoperability with Mellanox at PCI-SIG Developers Conference 2015 in Santa Clara, CA on June 23-24, 2015.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, complete interface IP solutions consisting of controller, PHY and next-generation verification IP, embedded processors and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit <http://www.synopsys.com/designware>.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP, and is also a leader in software quality and security testing with its Coverity® solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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