Synopsys Accelerates Automotive SoC Development with Broad Portfolio of Silicon-Proven IP

Availability of ASIL B Ready IP and Investment in AEC-Q100 Testing and TS 16949 Quality Management Accelerates Qualification of Automotive SoCs

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Highlights:

- DesignWare IP portfolio for automotive applications includes Ethernet AVB, LPDDR4, MIPI CSI-2 and DSI, HDMI, PCI Express, USB, Mobile Storage, Logic Libraries, Embedded Memories, NVM, Data Converters, ARC EM processors, EV vision processors and the Sensor and Control IP Subsystem
- ISO 26262 ASIL B Ready IP accelerates functional safety assessments to help designers reach target ASIL levels
- AEC-Q100 testing of IP reduces risk and development time for AEC-Q100 qualification of SoCs
- Development of IP that is compliant to the TS 16949 quality management specification helps meet the high quality levels required for automotive applications

Synopsys, Inc. (Nasdaq:SNPS) today announced that it is accelerating automotive SoC development with a broad portfolio of silicon-proven IP for automotive applications. The DesignWare® IP portfolio includes Ethernet Audio Video Bridging (AVB), LPDDR4, MIPI CSI-2 and DSI, HDMI, PCI Express®, USB, Mobile Storage, Logic Libraries, Embedded Memories, Non-Volatile Memories (NVM), Data Converters, Synopsys ARC® EM processors with Safety Enhancement Package (SEP), EV vision processors and the Sensor and Control IP Subsystem. The DesignWare IP portfolio meets key automotive functional safety requirements today and is being further enhanced to address AEC-Q100 and TS 16949 requirements. With DesignWare IP, SoC designers can accelerate their functional safety assessments and meet the high quality levels required in automotive applications such as advanced driver assistance systems (ADAS) and infotainment.

DesignWare Ethernet AVB, LPDDR4 and Embedded Memory IP are now certified to be ASIL B Ready for ISO 26262 functional safety, as required by ADAS applications. The ASIL B Ready DesignWare IP is delivered with safety packages that include failure modes effects and diagnostic analysis (FMEDA) reports as well as safety plans and manuals, giving designers the documentation needed to complete their own certification processes. By providing ASIL B Ready IP, Synopsys is helping designers reduce their development time and meet ISO 26262 functional safety requirements for their ADAS SoCs. In addition to the ASIL B Ready IP currently available, Synopsys offers ARC EM processors with SEP for safety-critical embedded applications and the ASIL D Ready ARC MetaWare Compiler.

"The market for semiconductors in automotive systems is forecasted to grow to$40.7 billion in 2021, with key drivers being ADAS and infotainment applications," said Colin Barnden, principle analyst at Semicast Research. "Developing applications such as pedestrian detection and lane departure warning and correction requires a new class of SoCs. By providing the necessary IP that has been certified to meet the functional safety standards, Synopsys enables SoC designers to more easily perform timely and successful safety-critical certification assessments, ultimately accelerating the qualification of their automotive SoCs."

"Functional safety, represented by ASIL B Ready certification, is crucial for new automotive applications such as ADAS," said Wolfgang Ruf, product manager at SGS-TUV Saar, a leading ISO 26262 training, testing and certification company. "Meeting ISO standards is key to demonstrating that an SoC, including its IP components, delivers enhanced processes for functional safety. By investing in the development of IP that meets strict certification guidelines, Synopsys is enabling SoC designers to more quickly meet their automotive design and certification objectives."

In addition to providing ASIL B Ready IP, Synopsys is making significant investments in IP solutions that are AEC-Q100 tested and meet TS 16949 quality management standards. The AEC-Q100 industry standard specification outlines the stress tests and reference test conditions for the qualification of automotive grade SoCs. By providing IP that is tested against applicable AEC-Q100 specifications, Synopsys is enabling designers to reduce design risk and development time for achieving SoC-level AEC-Q100 qualification. The TS 16949 quality management standard identifies risks in product development processes. By enhancing its IP development processes to fully support TS 16949 documentation requirements, Synopsys is providing the organization, policies, processes and resources needed to help designers meet SoC-level TS 16949 requirements.

"The growth of safety features in automotive SoCs requires IP providers to put strict processes in place to help ensure that the IP meets stringent functional safety standards," said John Koeter, vice president of marketing for IP and prototyping at Synopsys. "Our rich portfolio of DesignWare IP meets key automotive functional safety requirements today. We will continue to make significant investments in additional areas such as AEC-Q100 and TS 16949 to provide designers with a broad portfolio

of trusted IP solutions to help them accelerate the development and qualification of their automotive SoCs."

Availability & Resources

The following DesignWare IP is available now for automotive applications:

- ASIL B Ready Ethernet AVB, LPDDR4 and Embedded Memories
- ARC EM processors with Safety Enhancement Package (SEP) and the ASIL-D Ready ARC MetaWare Compiler
- Automotive Temperature Grade 0 qualified NVM IP

DesignWare MIPI CSI-2 and DSI, HDMI, PCI Express, USB, Mobile Storage, Logic Libraries, Data Converters, EV vision processors and the Sensor and Control IP Subsystem are being enhanced to support automotive-grade applications.

About DesignWare IP

Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, complete interface IP solutions consisting of controller, PHY and next-generation verification IP, embedded processors and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit http://www.synopsys.com/designware.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP, and is also a leader in software quality and security testing with its Coverity® solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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