Synopsys' IC Compiler II Used to Tape Out 28-nm-FD-SOI SoC

Delivers Game-Changing Benefits of 10X Faster Throughput

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Highlights:

- STMicroelectronics tapes out complex SoC design on 28-nm-FD-SOI technology using IC Compiler II
- Fast throughput and analysis delivered 10X reduction in time-to-good-floorplan
- 5X faster implementation with 2X smaller memory footprint enabled breakthrough productivity while exceeding QoR goals

Synopsys, Inc. (Nasdaq: SNPS) today announced STMicroelectronics, a global semiconductor leader serving customers across the spectrum of electronics applications, has taped out their latest fully depleted silicon on insulator (FD-SOI) system on chip (SoC) using Synopsys' IC Compiler™ II place and route solution.

Collaborating closely with Synopsys, ST used the tool to complete more than half of the chip, achieving higher designer productivity and better device performance. Unveiled in 2014, IC Compiler II is the successor to IC Compiler, the industry's current leading place and route solution for advanced design at established and emerging nodes. Driven by the FD-SOI tapeout success, ST is actively engaged in broadening the usage of IC Compiler II.

"Looking back, we can safely say it would have been exceedingly difficult to do a chip of this magnitude without IC Compiler II," said Thierry Bauchon, R&D Director at STMicroelectronics. "Our experience proved the promise we saw early in the design with 10X faster design exploration and 5X faster implementation, enabling us to refine floorplans, up-size physical partitions and achieve faster clock speeds on this tapeout."

IC Compiler II is a production-ready, full-featured place and route system architected from the ground-up to realize an order-of-magnitude leap forward in designer productivity. It is built on a new multi-threaded infrastructure able to handle designs with more than 500 million instances while continuing to utilize industry-standard input and output formats, as well as familiar interfaces and process technology files. Leveraging this new infrastructure, IC Compiler II offers ultra-high-capacity design planning, unique new clock-building technology and patented global analytical optimization, enabling enhanced quality of results (QoR) in area, timing and power. Representing years of engineering innovation and featuring several dozen new patents, these innovative technologies enable IC Compiler II to deliver 5X faster runtime along with half the memory and half the iterations required to achieve target QoR – all together enabling a 10X boost in design throughput. This level of speed-up is already enabling game-changing possibilities for IC Compiler II users and is continuing to transform how physical design is done.

"Over the years ST has been a steadfast partner helping us develop and deploy advanced design technology, and that has continued with our very latest offering, IC Compiler II," said Antun Domic, executive vice president and general manager of the Design Group at Synopsys. "The successful tapeout underscores the unique value IC Compiler II is delivering to a rapidly growing user base."

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP, and is also a leader in software quality and security testing with its Coverity® solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Editorial Contacts:
Sheryl Gulizia
Synopsys, Inc.
650-584-8635
sgulizia@synopsys.com

Lisa Gillette-Martin
MCA, Inc.

650-968-8900 ext. 115
lgmartin@mcapr.com

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