Synopsys Announces Industry's Lowest Power PCI Express 3.1 IP Solution for Mobile SoCs

Silicon-Proven, Compliant DesignWare IP Cuts Active Power Consumption to Less than 5 mW/Gb/Lane and Standby Power to Less than 10 uW/Lane

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Highlights:

- Power management features such as L1 sub-states and use of power gating, power islands and retention cells cut standby power to less than 10 uW/lane
- Support for supply under drive, a novel transmitter design and equalization bypass schemes reduce active power consumption to less than 5 mW/Gb/lane
- Offers small area, built-in at-speed production testing and optional wirebond packaging to lower overall BOM cost
- Reduces active power while meeting the PCI Express 3.1 electrical specification

Synopsys, Inc. (Nasdaq:SNPS) today announced the industry's lowest power controller and PHY IP solution for PCI Express® (PCIe®) 3.1 specification, significantly reducing both active and standby power consumption for mobile Systems-on-Chips (SoCs). The silicon-proven Synopsys DesignWare® IP for PCIe 3.1 specification incorporates L1 sub-states along with power gating techniques including the utilization of power switches, power islands or retention cells to reduce standby power to less than 10 uW/lane. In addition, supply under drive, a novel transmitter design and equalization bypass schemes cut active power to well below 5 mW/Gb/lane while meeting the PCIe 3.1 electrical specification. By providing a controller and PHY IP solution for PCIe technology that is optimized to deliver the lowest power consumption, Synopsys enables designers to incorporate the necessary functionality into their SoCs and extend the battery life of mobile devices.

"As a PCI-SIG member for more than a decade, Synopsys has helped advance PCIe technology," said Al Yanes, PCI-SIG chairman and president. "Products such as its low power IP solutions support the adoption of the PCIe architecture in SoCs used in mobile applications."

The DesignWare PHY IP for PCIe 3.1 technology exceeds required PCIe channel performance with multi-phase-locked loops (MPLLs), Feed Forward Equalization (FFE), Continuous Time Linear Equalization (CTLE) and programmable Decision Feedback Equalization (DFE) to enhance signal integrity across high loss and bumpy channels. Separate Refclk Independent SSC (SRIS), reference clock forwarding and PCI Express architecture aggregation and bifurcation provide flexibility and scalability for high-speed SoCs. The PHY's Automatic Test Equipment (ATE) test capabilities, small area and optional wirebond packaging reduce overall bill of materials (BOM) cost.

As part of the complete solution, the DesignWare Controller IP for PCI Express 3.1 specification supports L1 sub-states in conjunction with power islands or retention cells for up to 95 percent lower leakage power during standby mode and very low exit latency, enabling faster wake up time. To reduce active power, the controller supports system-level power management features including Latency Tolerance Reporting (LTR), Optimized Buffer Flush/Fill (OBFF) and Dynamic Power Allocation (DPA). In addition, Synopsys Verification IP (VIP) for the PCIe architecture combined with SystemVerilog source code test suites support the validation of low-power scenarios. The VIP provides controls to enter, switch between and exit low-power sub-states. It monitors low-power states, and the test suites provide a dedicated set of tests to validate L1 sub-states functionality.

"More features, faster performance and longer battery life are driving the evolution of mobile devices in the consumer electronics market," said John Koeter, vice president of marketing for IP and prototyping at Synopsys. "By providing the industry with the lowest power PCI Express IP solution, Synopsys is helping designers meet the stringent technology requirements of today's mobile applications and accelerate their time-to-market."

Availability
The low-power DesignWare Controller and PHY IP for PCIe 3.1 technology are available now. The Verification IP for PCIe 3.1 architecture as well as DesignWare IP Prototyping Kits for PCIe 3.1 Root Complex and for PCIe 3.1 Endpoint are also available now.

About DesignWare IP
Synopsys is a leading provider of high-quality, silicon-proven IP solutions for SoC designs. The broad DesignWare IP portfolio includes logic libraries, embedded memories, embedded test, analog IP, complete interface IP solutions consisting of

controller, PHY and next-generation verification IP, embedded processors and subsystems. To accelerate prototyping, software development and integration of IP into SoCs, Synopsys' IP Accelerated initiative offers IP prototyping kits, IP software development kits and IP subsystems. Synopsys' extensive investment in IP quality, comprehensive technical support and robust IP development methodology enables designers to reduce integration risk and accelerate time-to-market. For more information on DesignWare IP, visit http://www.synopsys.com/designware.

About Synopsys
Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP, and is also a leader in software quality and security testing with its Coverity® solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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Editorial Contacts:
Monica Marmie
Synopsys, Inc.
650-584-2890
monical@synopsys.com

Stephen Brennan
MCA, Inc.
650-968-8900, ext.114
sbrennan@mcapr.com

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