Synopsys' Verification IP for DDR4 3DS Enables DRAM Designs with Higher Density and Performance at Reduced Power

Native SystemVerilog-based VIP for DDR4 3DS Expands Synopsys' Portfolio of Memory VIP and Offers Built-in Coverage, Protocol Checks, Verification Plan and Protocol-aware Debug

MOUNTAIN VIEW, Calif., May 13, 2015 /PRNewswire/ -- Synopsys, Inc. (NASDAQ: SNPS) announces the availability of Verification IP (VIP) for the DDR4 3D Stacking (3DS) specification. Synopsys VIP for DDR4 3DS, based on its native SystemVerilog UVM architecture, is architected for ease of integration and configurability. The VIP for DDR4 3DS supports all JEDEC commands and provides pre-built DIMM (UDIMM, RDIMM, LRDIMM) models with protocol and timing checks, including support for memory vendor and the JEDEC standard part configurations. Synopsys' VIP for DDR4 3DS is natively integrated with its Verdi® Protocol Analyzer, offering a graphical protocol-aware debug environment that synchronizes memory transactions with signals. Complete with verification plans and built-in coverage, Synopsys' VIP for DDR4 3DS accelerates verification closure for designers of next-generation memory interfaces that require higher capacity and performance and reduced power to support enterprise computing devices, servers and data centers.

"The next generation of EZchip's multicore processors, the TILE-Mx, is optimized for high-performance networking applications and supports multiple DDR4 interfaces for up to 1TB of memory. A fundamental part of the new processor solution is high-performance and high-density DDR4 3DS LRDIMM," said Erez Shaizaf, director of VLSI at EZchip Semiconductor Ltd. "Synopsys VIP for DDR4 3DS is easy to use and provides the pre-defined LRDIMM model with comprehensive checks and coverage. The new VIP will enable us to close verification of the next-generation memory interfaces faster."

"As an active contributing member of the JEDEC, we have closely collaborated to develop DDR4 3DS VIP that allows leading-edge memory design teams to address the increasingly demanding process of protocol verification. The new VIP accelerates verification closure and time to market," said Debashis Chowdhury, vice president of R&D for the Synopsys Verification Group. "The release of Synopsys' VIP for DDR4 3DS demonstrates the results of our continued collaboration with SoC market leaders to enable increased design quality and faster, more complete verification closure."

Availability

Synopsys VIP for DDR4 3DS is available today, as well as being included in the Synopsys VIP Library and the Verification Compiler™ products.

About Synopsys Verification IP

Synopsys VIP, based on its next-generation architecture and implemented in native SystemVerilog, offers native performance, native debug with Verdi® Protocol Analyzer, enhanced VIP ease-of-use, configurability and coverage. These capabilities substantially increase user productivity for one of the most difficult and time-consuming aspects of SoC design and verification. The Synopsys VIP library includes a broad portfolio of interface, bus and memory protocols. More information is available at www.synopsys.com/vip.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP, and is also a leader in software quality and security testing with its Coverity® solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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