Synopsys' Modeling of 10-nanometer Parasitic Variation Effects Ratified by Open-Source Standards Board

Collaboration with Leading Semiconductor Companies and Foundries Delivers Silicon Accuracy with No Change in IC Design Analysis Flows

MOUNTAIN VIEW, Calif., April 21, 2015 /PRNewswire/ -- Synopsys, Inc. (Nasdaq: SNPS) today announced new extensions to its open-source Interconnect Technology Format (ITF) which enable modeling of complex device and interconnect parasitic effects at the advanced 10-nanometer (nm) process node. The new extensions include modeling of variation effects due to multi-patterning technology (MPT). Synopsys collaborated with the members of the Interconnect Modeling Technical Advisory Board (IMTAB) (member list available at www.imtab.org), an IEEE-ISTO Federation Member Program, to define and ratify these new extensions. They will be available in the upcoming open-source ITF version 2015.06.

"Enabling productive design and analysis for a colored layout flow, while also providing a solution to model increased parasitic variation due to MPT approaches, is critical at 10 nm," said Bari Biswas, vice president of engineering for extraction solutions at Synopsys and chair of IMTAB. "Through our collaboration with IMTAB members and leading foundries, Synopsys developed an innovative solution that extended the existing variation models in ITF to become intrinsically color-aware to more accurately model mask dependency while fitting seamlessly into a designer's existing flow."

"ITF continues to be the cornerstone of parasitic modeling in the semiconductor industry," said Marco Migliaro, President, IEEE-ISTO. "The new 10-nm models represent the fourth successive generation of model extensions fostered by the IMTAB consortium. IEEE-ISTO looks forward to continuing our support of the IMTAB mission to drive increased tool interoperability through the ITF common open-source modeling format."

MPT is an evolution of the double patterning technology (DPT) first introduced by foundries at the 20-nm process node, and it further extends the use of immersion lithography to 10 nm and below. However, MPT imposes tighter requirements on design implementation and analysis to support layout decomposition into different masks (coloring) and manage increased variation due to misalignment of the multiple masks. Synopsys' advanced MPT solution ratified by IMTAB for 10 nm includes color-aware models that cover all leading foundry manufacturing techniques including sequential litho-etch patterning, for example, triple patterning (LELELE) and quadruple patterning (LELELELE), as well as spacer-assisted/self-aligned patterning, for example, self-aligned double patterning (SADP) and self-aligned quadruple patterning (SAQP).

In addition to MPT modeling, Synopsys has introduced other ITF extensions approved by IMTAB for more accurate via resistance and device capacitance extraction at advanced FinFET process nodes. At 10nm, via resistivity has increased significantly with growing conductor environment context, so the existing self-aligned via resistance variation model has been extended to include coverage from top and bottom conductors. In addition, new ITF models have been added to accurately extract the floating gate to diffusion contact capacitance for polycide on diffusion edge (PODE) devices and spacer dielectric between gate polycide and contact, both of which are critical to regulating device performance.

More information on the new ITF extensions for 10nm can be found in the ITF specifications version 2015.06, targeted for release in June 2015.

Additional proposals for 10-nm and below process modeling are planned for review in the next IMTAB meeting scheduled for Tuesday, June 9, 2015 in San Francisco, CA, USA. The confirmation of the date and agenda for the meeting will be posted on the IEEE-ISTO's IMTAB website: www.imtab.org.

About ITF

Synopsys' Interconnect Technology Format (ITF) provides detailed modeling of interconnect parasitic effects that enables designers to perform accurate parasitic extraction for timing, signal integrity, power and reliability signoff analysis. ITF offers a flexible and innovative format to accurately model the effects of increased process variation at advanced process technologies. It is supported by leading semiconductor foundries, integrated device manufacturers and EDA tool providers.

ITF can be licensed for no charge through Synopsys' Technology Access Program (TAP-in^{SM} program). The latest specifications for ITF can be found at: www.synopsys.com/TapIn.

Requests for ITF enhancements come from the IMTAB membership as well as from the user community. Companies interested in IMTAB membership may contact IEEE-ISTO at imtab@ieee-isto.org.

About IEEE-ISTO

IEEE-ISTO is the premier trusted partner of the global technology community for the development, adoption and certification of industry standards. Its mission is to facilitate the life-cycle of industry standards development through a dedicated staff committed to offering vendor neutrality, quality support and member satisfaction. Fostering the market acceptance, adoption and implementation of standardized technologies, IEEE-ISTO programs span the spectrum of today's information and communications technologies. To find out more about IEEE-ISTO, visit www.ieee-isto.org.

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP, and is also a leader in software quality and security testing with its Coverity® solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Forward-looking Statements

This press release contains forward-looking statements within the meaning of Section 21E of the Securities Exchange Act of 1934, including statements regarding the expected release and benefits of the ITF specifications version 2015.06. These statements are based on current expectations and beliefs. Actual results, time frames or achievements could differ materially from those described by these statements due to risks and uncertainties including, but not limited to, unforeseen production or delivery delays, failure to perform as expected, product errors or defects, and other risks as identified in Synopsys' filings with the U.S. Securities and Exchange Commission, including those described in the "Risk Factors" section of Synopsys' latest Quarterly Report on Form 10-Q.

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