TSMC Certifies Synopsys Design Tools for 16-nm FinFET Plus Production and for 10-nm Early Design Starts

Synopsys Tools are 16-nm-Certified and Deployed in Production Designs; 10-nm Co-development Enables Engagements with Early Adopters

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Highlights:

- Certification includes the full suite of digital, signoff and custom implementation tools
- IC Compiler certification completed for 16-nm FinFET Plus v1.0 and the 10-nm (most current) version of the Design Rule Manual (DRM) and SPICE model
- IC Compiler II is under validation for 16FF+ v1.0, with certification targeted to be completed by the end ofApril 2015; certification of the 10-nm version of the DRM and SPICE model to be completed in June 2015

Synopsys, Inc. (Nasdaq: SNPS) today announced that TSMC has concluded 16-nanometer FinFET Plus (16FF+) v1.0 certification and reached the first milestone of 10-nanometer (nm) certification based on the most current DRM and SPICE model on a comprehensive list of Synopsys' custom and digital design tools. This certification enables mutual customers to deploy tools in Synopsys' Galaxy™ Design Platform for 16-nm production designs and 10-nm early engagements. The certified platform delivers technologies including routing rules, physical verification runsets, signoff-accurate extraction technology files, statistical timing analysis that correlates with SPICE, and interoperable process design kits (iPDKs) for FinFET processes. TSMC and Synopsys have collaborated to enhance new tool features based on both 16-nm and 10-nm technology requirements in Synopsys' IC Compiler™ II place and route solution with TSMC validation. This includes full-flow color enablement, support for connected poly on gate oxide and diffusion edge (CPODE) technology, layer optimization, low Vdd timing closure and support for signal electro-migration. The two companies are also working together to complete IC Compiler II certification for 16nm by the end of April and 10nm in June 2015.

"The combination of tool certification and our longstanding collaboration with Synopsys is enabling customers' 16FF+ production ramp-up and early engagements at 10-nanometer," said Suk Lee, TSMC Senior Director, Design Infrastructure Marketing Division. "With a full suite of TSMC-certified digital, signoff, and custom implementation solutions from Synopsys, our mutual customers will achieve improved performance and lower power while attaining their time-to-market goals."

"Our deep collaboration with TSMC on 16-nanometer and 10-nanometer FinFET processes allows our mutual customers to use silicon-proven FinFET tools to achieve predictable design closure with faster turnaround time," said Bijan Kiani, vice president of product marketing in Synopsys' Design Group. "With the latest certification for these two FinFET processes, designers can take advantage of this game-changing implementation technology for their next-generation chip designs."

Key Synopsys tools certified by TSMC include:

- IC Compiler II and IC Compiler: IC Compiler is fully certified for 16FF+ production and the most current DRM and SPICE model of 10-nm. IC Compiler II certification for 16FF+ production and the 10-nm early design starts will be completed by end of April 2015 and June 2015, respectively
- IC Validator: Fully color-aware signoff physical verification for FinFET designs
- StarRC™ extraction solution: Multi-patterning support, color-aware modeling and 3-D FinFET modeling
- PrimeTime® signoff solution: Signoff-accurate delay calculation and timing analysis with advanced waveform propagation includes impact of ultra-low voltage, increased Miller effect and resistivity, and process variations included in the standardized Liberty Variation Format (LVF) and multi-scenario ECO guidance to accelerate timing closure and leakage recovery
- PrimeRail: Accurate static and dynamic IR-drop analysis, color-aware electro-migration and power/ground (P/G) EM rules support
- NanoTime: SPICE-accurate transistor-level static timing analysis of 10-nm custom macros and embedded SRAMs
- DesignWare® STAR Memory System: Comprehensive test, repair and diagnostics solution for Synopsys and third-party embedded memories. Optimized memory test and repair algorithms provide high coverage of memory defects, including unique fault effects prevalent in FinFET-based memories
- Galaxy Custom Designer® schematic editor: Display mask color on schematic, assign color constraints and check schematics for color conflicts
- Laker® layout tool: Support for 10-nm full-coloring flow; reads color constraints from Galaxy Custom Designer schematic and enforces during layout; design-rule-driven color checking during layout and IC Validator integration to support color-

aware verification and color back-annotation
- HSPICE®, CustomSim™ and FineSim® simulation products: Support for 10-nm FinFET device modeling with self-heating effect and delivery of accurate circuit simulation results for the latest FinFET-based designs
- CustomSim also supports the latest design rules for electro-migration, IR-drop analysis and circuit electrical overstress (EOS) checking

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP, and is also a leader in software quality and security testing with its Coverity® solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

Forward-looking Statements

This press release contains forward-looking statements within the meaning of Section 21E of the Securities Exchange Act of 1934 regarding the expected release and benefits of IC Compiler II. Any statements that are not statements of historical fact may be deemed to be forward-looking statements. These statements involve known and unknown risks, uncertainties and other factors that could cause actual results, time frames or achievements to differ materially from those expressed or implied in the forward-looking statements. Other risks and uncertainties that may apply are set forth in the "Risk Factors" section of Synopsys' most recently filed Quarterly Report on Form 10-Q. Synopsys undertakes no obligation to update publicly any forward-looking statements, or to update the reasons actual results could differ materially from those anticipated in these forward-looking statements, even if new information becomes available in the future.

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