New Synopsys ASIP Designer Tool Speeds Development of Application-Specific Instruction-Set Processors by 5X

Automatic Generation of the Software Development Kit in Parallel with the Hardware Model Enables Rapid Architectural Exploration to Optimize ASIPs for Power, Performance and Area

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Highlights:

- Synopsys' ASIP Designer automates the design of application-specific instruction-set processors and programmable accelerators
- Leverages Synopsys' proven ASIP tool technology that has been used by more than 50 companies to design hundreds of successful products
- Unique "compiler-in-the-loop" feature enables use of application code to optimize ASIP architecture for performance and power
- Integrated LLVM-based compiler front-end and OpenCL kernel language support enables efficient compilation of C, C++ and OpenCL-based application code

Synopsys, Inc. (Nasdaq:SNPS) today announced availability of its new ASIP Designer tool that speeds the design of application-specific instruction-set processors (ASIPs) and programmable accelerators. ASIP Designer's language-based approach allows the automatic generation of synthesizable RTL and software development kits (SDKs) from a single input specification, accelerating the processor design and verification effort by up to 5X compared to traditional manual approaches. ASIPs are deployed in a wide range of signal-processing intensive applications, including wireless base stations, mobile handsets, audio processing, image processing and cloud computing.

"Using Synopsys' ASIP tools we've developed and deployed a full line of highly differentiated AudioSmart products. These products are based on the Conexant Audio Processing Engine, or CAPE, a Conexant-designed DSP," said Saleel Awsare, vice president and general manager at Conexant. "Application-specific architecture optimizations make CAPE highly efficient for far-field voice and audio playback processing, and Synopsys' tools assure ease of creation and programmability. By continuing to invest in ASIP tool technology, Synopsys is helping Conexant create market-leading domain-specific products."

ASIP Designer enables users to explore multiple processor architecture alternatives in minutes. Using a single input specification in the nML language, the tool automatically generates both the synthesizable RTL of the processor as well as an SDK that includes an optimizing C/C++ compiler, instruction set simulator, linker, assembler, software debugger and profiler. This ensures consistency of the hardware and the SDK at all stages of the design process. The patented compiler generation technology includes an LLVM compiler front-end and support for the OpenCL kernel language. Immediate availability of the compiler enables users to run their C, C++ and OpenCL application code on the automatically-generated instruction-set simulator as soon as the nML-based description is available. With this unique "compiler-in the-loop" approach as well as the extensive profiling capabilities of the debugger, ASIP Designer users can rapidly analyze and explore ASIP architectures and instruction sets to find the optimal power and performance design points for the target application.

ASIP Designer also automatically generates a SystemC-based transaction-level model, allowing pre-silicon software development using virtual prototypes such as those designed with Synopsys' Virtualizer™ tool set. A common and easy-to-use flow from RTL generation to instantiation in the HAPS® FPGA-based prototyping system, in addition to the automatic generation of JTAG-based on-chip debug logic, enables designers to integrate the ASIP into the system-on-chip (SoC) design and connect the prototype with real-world I/Os to validate the hardware-software integration.

A wide range of example ASIP designs for highly differentiated architectures, provided in nML source code, allows designers to quickly start designing their own ASIP that targets their specific application requirements.

"ASIPs offer distinct advantages over standard DSPs and fixed hardware in many data plane and signal processing applications," said John Koeter, vice president of marketing for IP and prototyping at Synopsys. "Synopsys' new ASIP Designer tool, built on proven technology used in hundreds of products in the market, helps design teams speed the development of custom processors and programmable accelerators tuned to their specific application. ASIP Designer gives users the ability to explore and optimize processor architectures for the best power, performance and area, giving them a distinct advantage in creating highly differentiated products."

Availability and Resources

Synopsys' ASIP Designer tool is available now. Learn more about Synopsys' ASIP Designer tool at

http://www.synopsys.com/ASIP

About Synopsys

Synopsys, Inc. (Nasdaq:SNPS) is the Silicon to Software™ partner for innovative companies developing the electronic products and software applications we rely on every day. As the world's 15th largest software company, Synopsys has a long history of being a global leader in electronic design automation (EDA) and semiconductor IP, and is also a leader in software quality and security testing with its Coverity® solutions. Whether you're a system-on-chip (SoC) designer creating advanced semiconductors, or a software developer writing applications that require the highest quality and security, Synopsys has the solutions needed to deliver innovative, high-quality, secure products. Learn more at www.synopsys.com.

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