# Synopsys Galaxy Design Platform Deployed by HiSilicon Technologies for Implementation of FinFET Designs

Successful Tapeouts Include the Newly Announced 64-bit ARM Cortex-A72 Processor-based SoC

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**Highlights:**

- Design Compiler Graphical and IC Compiler save several weeks of design time by minimizing iterations between synthesis and place and route
- IC Compiler achieves HiSilicon Technologies' aggressive power, performance and area targets and delivers predictable design closure
- PrimeTime ADV and IC Compiler enable single-pass timing and power ECO closure

Synopsys, Inc. (Nasdaq: SNPS) today announced that HiSilicon Technologies, a leading provider for telecom network, wireless terminal and digital media chipset solutions, has broadly deployed Synopsys' Galaxy™ Design Platform for the implementation of ARM® Cortex®-A72, Cortex -A57 and Cortex -A53 processor-based FinFET designs targeting TSMC's 16-nanometer (nm) process technology. The technology innovations for Synopsys in its Design Compiler® Graphical synthesis solution, IC Compiler™ place and route tool, PrimeTime® ADV advanced timing closure tool, StarRC™ extraction solution and IC Validator physical verification tool were instrumental in enabling multiple production tapeouts of industry-leading performance, low-power, multi-core designs implemented by HiSilicon Technologies.

"We have selected the Galaxy Design Platform for all of our FinFET implementation because of the superior quality of results delivered by the platform," said Yu Lin, senior director of Technology Platform Engineering at HiSilicon Technologies. "A strong collaboration with Synopsys has enabled us to meet our production tapeout milestones for all Cortex-A Series designs in a timely and predictable manner. We are broadly deploying the platform to achieve superior results."

In collaboration with Synopsys, HiSilicon Technologies recently completed a 16-nm production tapeout that contained more than 50 million instances, including four ARM Cortex-A72 quad-core processor clusters, each measuring 1.6 million instances. The move from planar (bulk) to tri-gate (FinFET) devices and the use of double patterning technology (DPT) can be a disruptive transition, but Synopsys worked closely with HiSilicon Technologies to develop a robust 16-nm design implementation methodology that includes several key technologies from the Galaxy Design Platform:

- Physical guidance from Design Compiler Graphical enables tight correlation with IC Compiler, saving up to three weeks of design time;
- Layer-aware optimization in Design Compiler and IC Compiler, together with concurrent clock and data optimization in IC Compiler, increases design performance;
- Variation-aware multisource clock tree synthesis technology in IC Compiler provides low skew and latency;
- Advanced net and device delay models, including resistive shielding on long nets and waveform propagation, enable modeling of signal distortion and tighter silicon correlation;
- FinFET grid placement and route rule support enable quick and reliable 16-nm manufacturing compliance with IC Compiler and IC Validator;
- Advanced parasitic extraction delivers signoff accuracy with StarRC;
- PrimeTime ADV physically aware engineering change order (ECO) guidance with IC Compiler provides faster ECO closure and power recovery.

"We are committed to enabling industry leaders such as HiSilicon Technologies to achieve aggressive design targets and production milestones," said Antun Domic, executive vice president and general manager, Synopsys Design Group. "The Galaxy Platform's proven track record of technology innovations for high-performance design and our decade-long collaboration with the FinFET ecosystem was instrumental to the success of this production tapeout."

**About Synopsys**

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