Synopsys' IC Compiler II Enables Toshiba's Tapeout of Complex 40-nm SoC, Proves out Game-Changing Capabilities

Toshiba Standardizes on IC Compiler II for Physical Design

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Highlights:

- IC Compiler II enables Toshiba's successful tapeout of advanced 40-nm SoC
- 6X faster design turnaround time with one-third of the memory footprint
- 60 percent smaller buffer area during clock tree synthesis delivers superior design area and power QoR
- Seamless handling of multiple modes and corners reduces timing ECO iterations

Synopsys, Inc. (Nasdaq: SNPS) today announced that its IC Compiler[™] II place and route solution has enabled Toshiba to accelerate tapeout of an advanced 40-nanometer (nm) system on chip (SoC). The impressive speedup and superior QoR delivered by IC Compiler II enabled Toshiba to achieve higher designer productivity and better device performance. Unveiled less than a year ago, IC Compiler II is the successor to IC Compiler, the industry's leading place-and-route solution for advanced design at established and emerging nodes. Driven by this tapeout success, Toshiba has commenced the immediate rollout of their IC Compiler II-based design kit throughout their design teams.

"We are extremely impressed with the unprecedented runtime speedup and superior QoR delivered by IC Compiler II on this tapeout," said Mr. Kazunari Horikawa, senior manager of Design Technology Development Department, Mixed Signal IC Division at Toshiba Corporation Semiconductor and Storage Products Company. "The ultra-fast implementation turnaround times enabled daily iterations on this complex SoC, allowing us to exceed our QoR goals. We have released our IC Compiler II based design kit to commence standardization on IC Compiler II to enable other critical designs within Toshiba to benefit from these game-changing capabilities."

IC Compiler II is a production-ready, full-featured place-and-route system architected from the ground-up to realize an order-of-magnitude leap forward in designer productivity. It is built on a new multi-threaded infrastructure that is able to handle designs with more than 500 million instances while continuing to utilize industry-standard input and output formats, as well as familiar interfaces and process technology files. Leveraging this new infrastructure, IC Compiler II offers ultra-high capacity design planning, unique, new clock-building technology and patented global analytical optimization, enabling enhanced area, timing and power QoR. Representing years of engineering innovation and featuring several dozen new patents, these innovative technologies enable IC Compiler II to deliver 5X faster runtime along with half the memory and half the iterations required to achieve target QoR – all together enabling a 10X boost in design throughput. This level of speed-up is already enabling game-changing productivity for IC Compiler II users and is continuing to transform how physical design is done.

"Toshiba joins the growing list of companies who are adopting IC Compiler II," said Antun Domic, executive vice president and general manager of the Design Group at Synopsys. "The successful tapeout of this highly complex SoC and Toshiba's decision to subsequently expand the usage to other programs with their design kit underscores the unique value IC Compiler II is delivering to a rapidly growing user base."

About Synopsys

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